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12 CMOS Transimpedance Amplifiers for Biomedical Applications: A Comparative Study

Ahmed Atef, Mohamed Atef, Elsayed Esam M. Khaled, and Mohamed Abbas

Recently, different medical devices have emerged and utilized in a numerous health care fields such as pulse oximetry, cuffless blood pressure using Photoplethysmogram (PPG), noninvasive blood glucose measuring, and Near Infrared Spectroscopy (NIRS). Those devices are very similar in their analog front end circuit which is a transimpedance amplifier (TIA). Many different TIA topologies have appeared in different optoelectronic fields which make the choice of the best TIA topology for a certain application a challenging task. In this regard, this paper presents a comparison between state of the art, previously published TIA topologies. All topologies are simulated at four different simulation cases to account for various design scenarios. The topologies are simulated with 10 pF photodiode (PD) input capacitance and 5 kHz bandwidth (BW) while optimizing for two different targets; one time for minimum input noise and the other for minimum power consumption. Moreover, the same procedures are performed with 2 pF PD and 100 MHz BW to account for higher BW demanding applications. The studied topologies are compared according to their transimpedance gain, power consumption, total input referred noise current, and dynamic range (DR) to expose their relative merits. A noise and a transimpedance gain mathematical models are also presented for each topology to assist the comparison. Recommendations to designers on which TIA to select in a certain application are concluded according to the obtained results.

32 An Alternative Path to Foster's Reactance Theorem and Its Relation to Narrow-Band Equivalent Circuits

Bernhard Jakoby

Foster's seminal treatise on lossless networks has been published almost 100 years ago and a particularly notable conclusion drawn therein, i.e. that the reactance (and susceptance) functions are always monotonically increasing with frequency, is frequently referred to as Foster's theorem. In this paper we present two variants for an alternative simple derivation of a stronger form of this theorem, which holds for the driving point reactance (susceptance) of general lossless devices, i.e. also configurations without lumped elements. One version introduces a realizable lumped element equivalent circuit approximating the considered circuit in a narrow band around a particularly considered frequency. It turns out that this avenue of proof also facilitates an alternative validation of the realizability of the so called Foster 1 and 2 realizations.

40 Adapted Compressed Sensing: A Game Worth Playing

Mauro Mangia, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti

Despite the universal nature of the compressed sensing mechanism, additional information on the class of sparse signals to acquire allows adjustments that yield substantial improvements. In facts, proper exploitation of these priors allows to significantly increase compression for a given reconstruction quality. Since one of the most promising scopes of application of compressed sensing is that of IoT devices subject to extremely low resource constraint, adaptation is especially interesting when it can cope with hardware-related constraint allowing low complexity implementations. We here review and compare many algorithmic adaptation policies that focus either on the encoding part or on the recovery part of compressed sensing. We also review other more hardware-oriented adaptation techniques that are actually able to make the difference when coming to real-world implementations. In all cases, adaptation proves to be a tool that should be mastered in practical applications to unleash the full potential of compressed sensing.

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- 7 CAS Society News

Scope: Insofar as the technical articles presented in the proposed magazine, the plan is to cover the subject areas represented by the Society's transactions, including: analog, passive, switch capacitor, and digital filters; electronic circuits, networks, graph theory, and RF communication circuits; system theory; discrete, IC, and VLSI circuit design; multidimensional circuits and systems; large-scale systems and power networks; nonlinear circuits and systems, wavelets, filter banks, and applications; neural networks; and signal processing. Content will also cover the areas represented by the Society technical committees: analog signal processing, cellular neural networks, and array computing, circuits and systems for communications, computer-aided network design, digital signal processing, multimedia systems and applications, neural systems and applications, nonlinear circuits and systems, power systems and power electronics and circuits, sensors and micromachining, visual signal processing and communication, and VLSI systems and applications. Lastly, the magazine will cover the interests represented by the widespread conference activity of the IEEE Circuits and Systems Society. In addition to the technical articles, which may be seen as the centerpiece of the start-up plan, we plan also to cover Society administrative activities, as for instance the meetings of the Board of Governors, Society People, as for instance the stories of award winners-fellows, medalists, and so forth, and Places reached by the Society, including readable reports from the Society's conferences around the world.

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Yiran Chen, Ph.D.

The Editor in Chief of IEEE Circuits and Systems Magazine

2020: Looking Forward to the Next Decade

2020 is the Year of the Rat according to Chinese zodiac. It is also the first in the zodiac cycle, representing agility, flexibility, and adaptability. Standing at the transition point between two decades, we have never been facing so many exciting challenges and opportunities, which will greatly reform the future of circuits and systems, and change our daily life.

Artificial Intelligence (AI) is unarguably the hottest technology in the past decade. Data, algorithm, and computing form the three cornerstones of AI. Indeed, it was the appearance of powerful computing systems (e.g., the application of GPU in deep neural network training) that triggered the upsurge of AI technology. Many new chips have been designed to accelerate the training and execution of AI algorithms, and expedite the deployment of AI systems. Innovative architectures such as process-in-memory (PIM), analog computing, neuromorphic computing were proposed to break the limits of von Neumann architecture. Emerging devices, such as resistive memory and spintronic memory, have been also adopted in these practices to explore new scaling paths of post-CMOS era.

Quantum computing is another transformative technology in circuits and systems. Solid progress has been made in the past several years and we are getting closer and closer to so called “quantum supremacy”. A relevant technology—superconducting circuits, has also promised two orders of magnitude energy efficiency

and clock frequency compared to state-of-the-art CMOS circuits.

IEEE Circuits and Systems Magazine (CAS-M) is ready to become more agile, flexible, and adaptive to embrace these technology trends and prepare for a new decade. The newly formed editorial board is particularly strengthened the expertise in many emerging technology directions. We hope that CAS-M can serve as the central hub of the members of IEEE Circuits and Systems (CAS) society to learn new knowledge, communicate with other members, share their technical thoughts and opinions, and cultivate the new-generation circuits and systems engineers.

Last but not least, I would like to take this opportunity to thank the dedication of the editorial board of 2016–2019 in the past four years. Because of their diligent works, CAS-M now has become the periodical of IEEE CAS with the highest impact factor. The success of CAS-M is also due in large part to the leadership of Dr. Chai Wah Wu, the Editor in Chief of the last editorial board, the strong support from IEEE periodical editorial and production service team, and the active participations of all the authors and reviewers. We invite everybody to continue submitting articles, news, and correspondence to CAS-M and hope that the magazine will continue to be a stimulating and useful resource to the members of IEEE CAS for many years to come.

Wish everybody a joyous, healthy, and prospectus 2020!

A handwritten signature in black ink, appearing to read 'Yiran Chen'.

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Amara Amara

President, IEEE Circuits and Systems Society (2020–2021)

I would like first, to pay tribute to the presidents who preceded me and who made our society a dynamic one, among the most agile and have established remarkable financial health that enables us to support our chapters and our members through many initiatives.

It is with great pride that I begin my term as President of our Society. I am aware of the heavy responsibility I will have, and I am sure that I can count on a collaborative spirit with all of the colleagues from the ExCom and the BoG as well as the active support of our members.

I have just finished my term as President Elect during which I engaged myself and my colleagues from the Executive Committee, the BoG and the Long-Term Strategy Committee in the elaboration of a strategic plan 2020–2024. During this development process, we revised our mission and our vision, aligned with the United Nations priorities also known as the Sustainable Development Goals (SDGs). Our society has a broad technical and scientific spectrum enabling it to cover most of these SDGs.

In addition to the revision of the mission and the vision, we have also defined a set of values: scientific excellence, inclusion and participation and service to humanity to name only a few.

This reflection also led us to define both global and technical strategic areas.

Concerning the global strategic areas, the service to our members is the main priority. Going beyond our borders will allow us to reach out to other categories of populations that are little or not at all represented and finally focusing on technical excellence and inspiration will establish the leadership of our Society in new emerging areas of circuits and systems.

Regarding the technical strategic areas, we have classified them into three complementary categories:

1. New paradigms governing the engineering of Circuits and Systems encompassing interfacing, computation, and connectivity
2. Applications of Circuits and Systems including food and agriculture, healthcare and livelihood,

human-centric technology, mobility, and smart cities and sustainable energy

3. The fundamental theory supporting emerging technologies

An in-depth analysis of the SWOT and the TOWS allowed us to define three strategic initiatives for each division (technical activities, publications, conferences, and regional activities and membership) which will constitute the frameworks of the annual operational plans of each division, details will be published on our website very soon.

To facilitate the achievement of our strategic plan we will rely on 3 main levers.

1. Development of proximity with our members by meeting them at their place, by directly discussing with them their challenges and expectations
 2. Digital communication plan with an increased presence in social networks
 3. Outreach and growth of our activities in geographic areas such as Africa and Southeast Asia
- Therefore we are going to launch several initiatives in January:

- Africa initiative
- Regional CASS Days following the successful Europe CASS Day
- Entrepreneurship initiative in connection with the SDGs
- Global education by reorganizing this activity within a Global Education Institute including the DLP and iDLP (industry DLP) programs
- Seasonal Schools, Microlearning, e-books etc.

The content generated will be made available to our members free of charge in our resource center.

In addition, this body could be endowed with more prerogatives and governance which will be discussed within the ExCom and the BoG during this year.

To conclude, I would like to thank members of the ExCom and the BoG who finished their terms and welcome the new members. I count on the commitment of all the members of the ExCom, the BoG, the technical activities committees and all the Chapter officers to help in the implementation of our strategic plan.



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Sanjit Mitra Elected to National Academy of Inventors Fellow

Prof. Sanjit K. Mitra of UC Santa Barbara was elected to National Academy of Inventors (NAI) Fellow status. The NAI Fellows Program was established to highlight academic inventors who have demonstrated a prolific spirit of innovation in creating or facilitating outstanding inventions that have made a tangible impact on quality of life, economic development and the welfare of society. Election to NAI Fellow status is the highest professional distinction accorded solely to academic inventors.

Prof. Mitra is a Fellow of the IEEE and past CASS president. He has published more than 700 papers in the areas of analog and digital signal processing, and image processing. He also authored and co-authored twelve books and holds six patents. Dr. Mitra is the recipient of the 2000 IEEE Mac Van Valkenburg award and the 2006 Education Award of the IEEE Signal Processing Society, the IEEE Millennium Medal in 2000, the McGraw-Hill/Jacob Millman Award of the IEEE Education Society in 2001, the 2006 IEEE James H. Mulligan, Jr. Education Medal, and the 2013 IEEE Gustav Robert Kirchhoff Award. He has been awarded Honorary Doctorate degrees from the Tampere University of Technology, Finland, the Technical University of Bucharest, Romania, and the Technical University of Iasi, Romania.

New IEEE Fellows

Members of CASS and Evaluated by CASS

Alyssa Apsel, *for contributions to radio frequency and optical communications circuits and systems*

Ramon Carvajal, *for contributions to low-voltage and low-power CMOS analog circuit design*

Sen-ching Cheung, *for contributions to multimedia data processing and their applications in autism interventions*

Jose De La Rosa, *for contributions to delta-sigma modulators*

Ramesh Karri, *for contributions to and leadership in trustworthy hardware*

Huazhong Yang, *for low-power circuit techniques for sensor applications and design automation*

Lei Zhang, *for contributions to large-scale visual recognition and multimedia information retrieval*

Tong Zhang, *for contributions to system design and VLSI implementation for data storage.*

Members of CASS and Evaluated by Other IEEE Entities

William Bidermann, *for leadership in commercially successful image sensors and microprocessors*

Kawai Cheng, *for contribution to electric vehicle technology and switched-capacitor power conversion*

Maciej Ciesielski, *for contributions to logic synthesis and formal verification of arithmetic circuits*

Ravinder Dahiya, *for contributions to tactile sensing*

Touradj Ebrahimi, *for contributions to visual information representation and assessment of quality of experience in multimedia*

Christoforos Hadjicostis, *for contributions to distributed and discrete event systems*

Pavan V Hanumolu, *for contributions to the design of mixed-signal integrated circuits*

Eric A M Klumperink, *for contributions to thermal noise cancelling and software defined radio architecture*

Yiannos Manoli, *for contributions to the design of integrated analog-to-digital interface circuits and energy harvesting systems*

Partha Pande, *for contributions to network-on-chip architectures for manycore computing*

Michael Perrott, *for contributions to phase-locked loop integrated circuits*

Yonggang Wen, *for contributions to cloud systems for multimedia signal processing and communications*

Yonghong Zeng, *for contributions to spectrum sensing and medium access control in cognitive radio.*

CAS Society News

Santa Clara Valley Chapter

IEEE Circuits and Systems Society (CASS) held a technical lecture on April 11th 2019 titled “Enabling Wireless Autonomous Systems Using 5G” given by Dr. Nageen Himayat who is the Director of Intelligent

Distributed Edge Networks Labs at Intel. The total attendance was 51. Dr. Himayat articulated on the huge economic and societal impact of Autonomous Wireless Systems (WAS) while outlining significant challenges in meeting the reliability, latency and scalability requirements of these safety critical applications. On April 25th, Dr. Alyssa Apse (CASS DL) from Cornell University

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Lecture with Dr. Nageen Himayat. From left to right, George Chen (Secretary), Robert S. Ogg (Advisor), Nageen Himayat (Intel), Imran Bashir (Chair), Johnathan David (Advisor), Mojtaba Sharifzadeh (SSCS-Chair).



CASS Lecture with Dr. Alyssa Apse “Flexible Radios and Flexible Network.” From left to right, Mojtaba Sharifzadeh (SSCS-Chair), Robert S. Ogg (Advisor), Julian Tham (Cypress), Dr. Alyssa Apse (CASS DL), Amit Jha (Vice Chair).

gave a lecture titled “Flexible Radios and Flexible Networks.” In her lecture, Dr. Apsel described various approaches to drive the power down in radio networks that span across circuits and systems while adding flexibility to adapt across protocols and networks and work under changing device technologies. The total attendance was 28. On September 6th, the Artificial Intelligence for Industry (AI4I) Fall 2019 was held at SC-9

Auditorium, Intel in Santa Clara. This half day sold-out event hosted four speakers and the total attendance as 148. The first speaker of the event was Dr. S. Y. Kung from Princeton University and the title of his lecture was “From Deep Learning to X-Learning: An Internal and Explainable Learning for XA.” In his talk, Dr. Kung described an Xnet that is used to simultaneously train the structure and parameters of the net while facilitating



CASS Lecture event with Dr. Waleed Khalil, “VCO Design Challenges and Solutions for mm-Wave Applications.”



CASS AI4I Forum Fall 2019. Pete Warden (Google) receiving a certificate from CASS.



CASS AI4I Forum Fall 2019. Jianhui Li (Intel) answering questions from the audience.



CASS AI4I Forum Fall 2019. View of the lecture hall at SC-9 Intel, Santa Clara during the event.



CASS AI4I Forum Fall 2019. Ephrem Wu (left) receiving a certificate from Tong Zhang (Intel, AI4I event organizer).



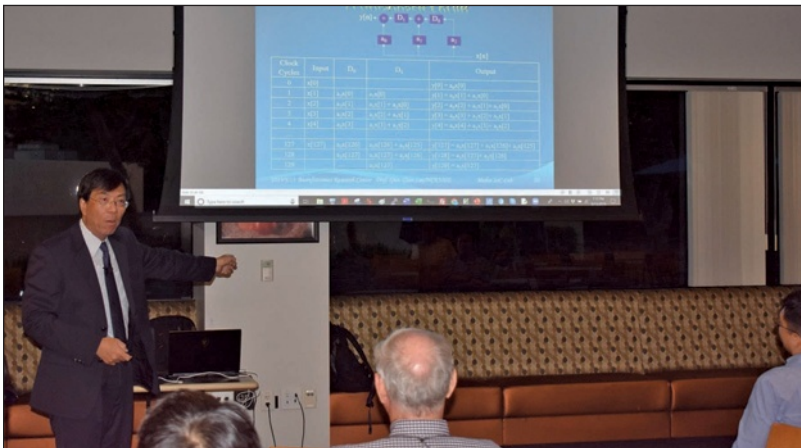
CASS Lecture event with Dr. Christopher Hull, "Millimeter-Wave Power Amplifiers in FinFET Technology."



CASS Lecture event with Dr. Claude Gauthier, "Automotive Ethernet and Functional Safety."



CASS DL Event with Dr. Shanti Pavan “Dissecting Design Choices in Continuous-time Delta-Sigma Converters”. From left to right, George Chen (CASS-Secretary), Jonathan David (Advisor), Amit Jha (CASS-Vice Chair), Dr. Shanti Pavan (CASS DL), Robert S. Ogg (Advisor).

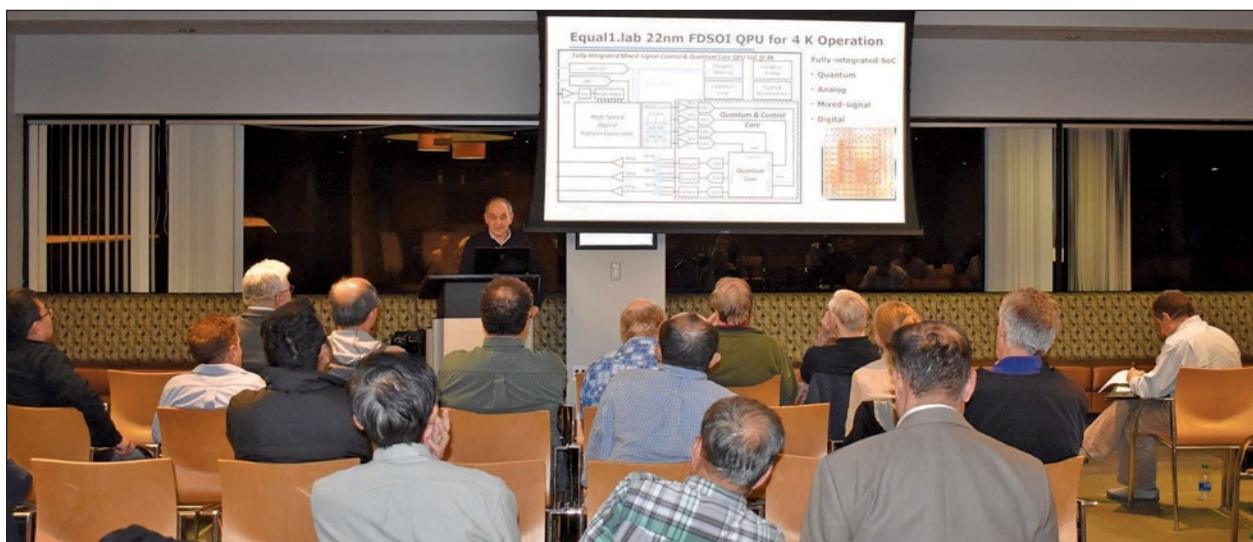


CASS Distinguished Lecturer event with Dr. Chris Guo Giun, “Algorithm/Architecture Co-design for Smart Signals and Systems In Cognitive Cloud/Edge.”



CASS AI4I Forum Fall 2019. Dr. S. Y. Kung giving a lecture on Xnet.

Internal Neuron’s Explainability so as to fully support DARPA’s Explainable AI (i.e. XAI or AI3.0). This is a superior approach when compared to Back-propagation (BP), an external learning paradigm, whose supervision is exclusively accessed via the external interfacing nodes (i.e. input/output neurons). The second speaker of the forum was Pete Warden (Google) who covered the emerging requirements of deep learning workloads, including the barriers that are preventing more widespread deployment on low-energy systems. The third speaker of the forum was Ephrem Wu who is a Sr. Director in the Silicon Architecture division at Xilinx. Ephrem outlined the performance requirements of FPGA-based neural-network accelerators and the strategies for meeting those challenges. The fourth and last speaker of the forum was Jianhui Li who is a Principal Engineer at Intel. In his talk Jianhui analyzed deep learning algorithms from compute performance perspective and discussed how key software optimizations unleash the power of AI hardware from the cloud to the edge. On September 13th, Dr. Chris Gwo Giun (CASS DL) gave a lecture titled “Algorithm/Architecture Co-Design for Smart Signals and Systems In Cognitive Cloud/Edge” and the total attendance was 17. Dr. Chris Gwo Giun introduced the concept of concurrent exploration of algorithm and architecture entitled Algorithm/Architecture Co-exploration (AAC). This methodology introduces a paradigm shift in advanced system design from System-on-a-Chip to Cloud and Edge as algorithms with high accuracy become exceedingly more complex and Edge/IoT generated data becomes increasingly bigger. Dr. Shanti Pavan (CASS DL) gave a lecture on September 26th “Dissecting Design Choices in Continuous-time Delta-Sigma Converters” and the total attendance was 40. In his talk, Dr. Pavan gave a survey of alternatives for the design of power efficient single-loop continuous-time



CASS Lecture Event with Dr. Sorin P. Voinigescu, “Towards monolithic quantum computing processors in production FDSOI CMOS technology.”

delta sigma converters while underscoring their unique features, differences and specifications. Dr. Christopher Hull (Intel) gave a lecture titled “Millimeter-Wave Power Amplifiers In FinFET Technology” on October 16th and the total attendance was 42. Dr. Hull gave an overview of specifications for fifth generation cellular communications standards (5G) targeting Gb/s data-rates and the benefits of CMOS FINFET technology when it comes to integration and scaling. A major portion of the lecture was dedicated to the circuit design process and challenges. On November 1st, Dr. Waleed Khalil gave a lecture titled “VCO Design Challenges and Solutions for mm-Wave Applications” and the total attendance was 32. The lecture generated lots of Q&A and interest from the audience. On December 12th, Dr. Sorin P. Voinigescu

gave a lecture titled, “Towards monolithic quantum computing processors in production FDSOI CMOS technology” and the total attendance was 40. Dr. Voinigescu gave a brief introduction to quantum computing and covered various processors and published qubit technologies and their trade-offs. CASS now has its own channel on IEEE TV for streaming of previously recorded lectures (Google “IEEE TV Circuits and Systems”). Please visit the chapter’s website @ <http://sites.ieee.org/scv-cas> and join the email list to receive notification of future events and instructions on joining remotely through Zoom. If you have any feedback or suggestions, please email the chapter leadership at: ieee.scv.cas@gmail.com.

Many thanks to Imran Bashir who contributed to this report.





CMOS Transimpedance Amplifiers for Biomedical Applications: A Comparative Study

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Abstract

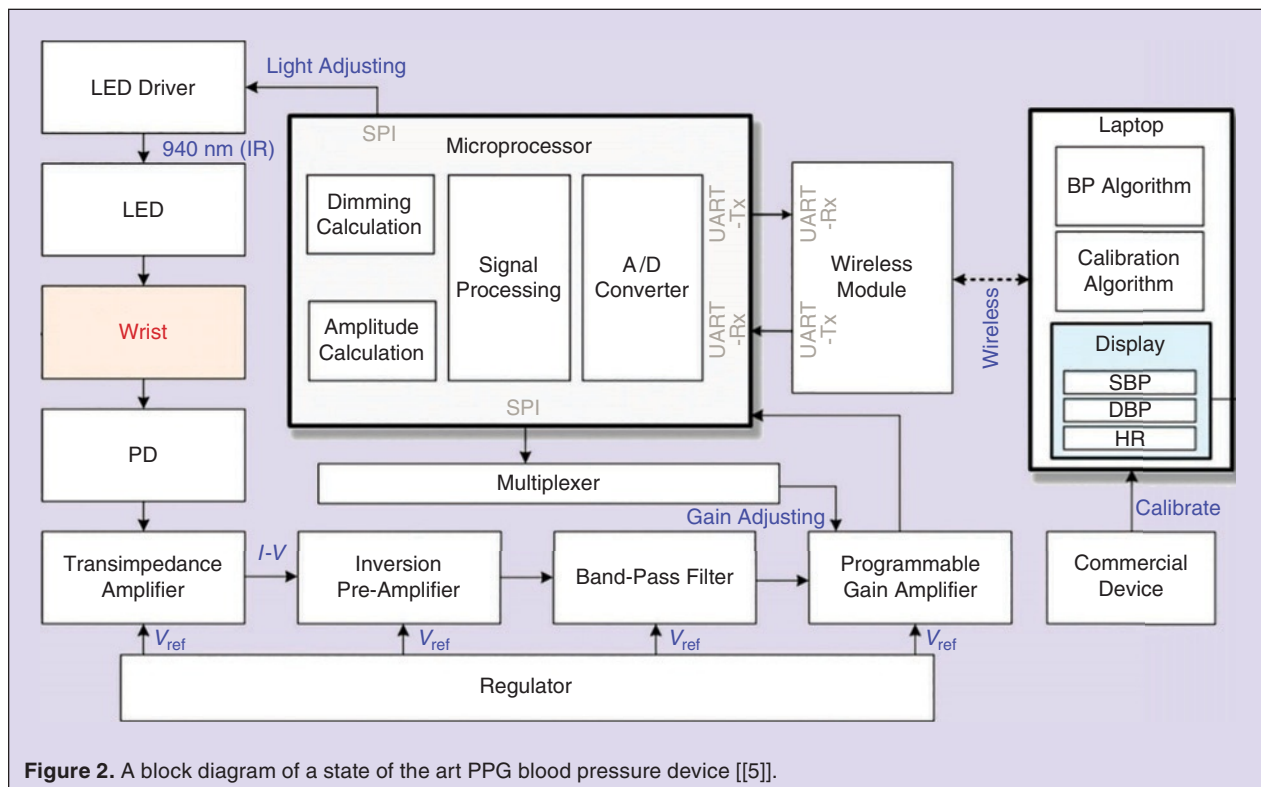
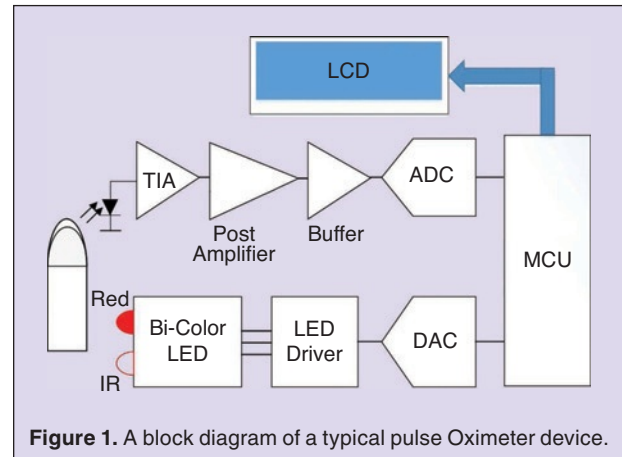
Recently, different medical devices have emerged and utilized in a numerous health care fields such as pulse oximetry, cuffless blood pressure using Photoplethysmogram (PPG), noninvasive blood glucose measuring, and Near Infrared Spectroscopy (NIRS). Those devices are very similar in their analog front end circuit which is a transimpedance amplifier (TIA). Many different TIA topologies have appeared in different optoelectronic fields which make the choice

of the best TIA topology for a certain application a challenging task. In this regard, this paper presents a comparison between state of the art, previously published TIA topologies. All topologies are simulated at four different simulation cases to account for various design scenarios. The topologies are simulated with 10 pF photodiode (PD) input capacitance and 5 KHz bandwidth (BW) while optimizing for two different targets; one time for minimum input noise and the other for minimum power consumption. Moreover, the same procedures are performed with 2 pF PD and 100 MHz BW to account for higher BW demanding applications. The studied topologies are compared according to their transimpedance gain, power consumption, total input referred noise current, and dynamic range (DR) to expose their relative merits. A noise and a transimpedance gain mathematical models are also presented for each topology to assist the comparison. Recommendations to designers on which TIA to select in a certain application are concluded according to the obtained results.

I. Introduction

The rapid technological growth of CMOS bioelectronics integrated circuits have enhanced health care in many different ways. Nowadays, optoelectronics integrated circuits design is considered as one of the most rapidly evolving research topics. Pulse oximetry is one of the early methods emerged on the health care field that uses optoelectronics integrated circuits, see Fig. 1. It utilizes

two wavelengths (IR and Red) to measure pulsating arteries blood oxygen saturation [1]. Another revolutionary technique that relays on optoelectronics which is currently under developing and testing is the cuffless blood pressure measurement using photoplethysmogram (PPG) [2]–[4]. Fig. 2 shows a block diagram of a state of the art handheld PPG based cuffless blood pressure device [5].



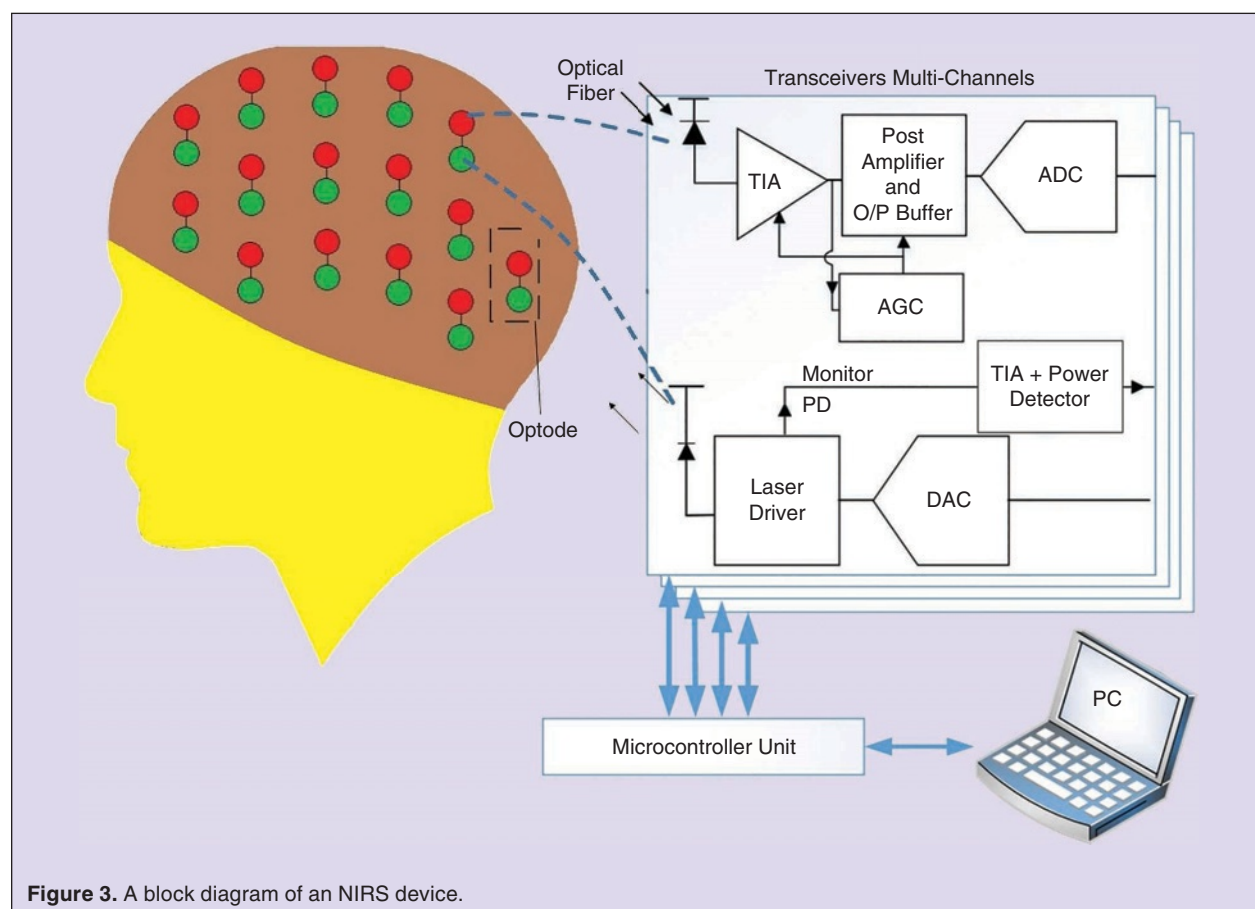
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In addition, different researches have investigated the ability to measure blood glucose level noninvasively using optoelectronics methods [6]–[9]. Furthermore, Near Infrared Spectroscopy (NIRS) is a state of the art technique that uses optoelectronics in which multiple near infrared wavelengths are employed to measure different brain blood chromophores like hemoglobin, oxy-hemoglobin and cytochrome c-oxidase [10]–[14]. A block diagram describing the building construction of an NIRS system is shown in Fig. 3. NIRS has many current and future applications like brain function mapping [15], [16], epilepsy seizure prediction [17], lung efficiency assessment [18], and preventing hypoxia in open heart surgeries [19], [20]. Those mentioned optoelectronic devices in Fig. 1, 2 and 3 are very similar in their circuit architecture; they transmit an optical signal to the human tissues and detect the reflected signal with a photodiode (PD).

In all of the previously mentioned biomedical devices, a PD converts the optical power into an electrical photocurrent which is fed to a transimpedance amplifier (TIA) for amplification and conversion to an output voltage. Two stages, a post amplifier and an output buffer, are usually included in all of the mentioned previously biomedical devices.

There are many TIA topologies presented in the literatures. Each is designed for a certain biomedical application. Consequently, the main challenge facing every optoelectronic circuit designer is how to choose a suitable TIA topology for the intended biomedical application regarding many aspects such as the transimpedance gain, BW, input referred noise current, power consumption, and dynamic range. Some of those aspects may be in a direct trade-off with each other making the choice even more challenging. Accordingly, this paper presents an analysis, simulation, and comparison of eight different state of the art TIA topologies helping the designer to find the appropriate TIA that meets their requirements.

The investigated TIAs topologies in this study, including overall analysis, simulation, and comparisons, are the common source TIA (CS-TIA) [21]–[24], the inverter based TIA (Inv-TIA) [25]–[28], the inverter cascode based TIA (InvCas-TIA) [29], the regulated inverter cascode (RIC-TIA) [30], [31], the current reuse TIA (CR-TIA) [32], [33], the current reuse with regulated cascode TIA (CR-RGC-TIA) [34], the common gate TIA (CG-TIA) [35], and the regulated cascode TIA (RGC-TIA) [22], [36]–[38]. All of the investigated topologies are simulated using 130 nm standard CMOS technology with the same 1.2 V



DC supply voltage. Moreover, each TIA is simulated while targeting four different cases, those cases can be summarized as follows:

- 1) 10 pF PD capacitance and 5 KHz BW while targeting minimum input referred noise.
- 2) 10 pF PD capacitance and 5 KHz BW while targeting minimum power consumption.
- 3) 2 pF PD capacitance and 100 MHz BW while targeting minimum input referred noise.
- 4) 2 pF PD capacitance and 100 MHz BW while targeting minimum power consumption.

Since the detected optical signal is very weak, a large area integrated PD has to be used to collect most of the reflected optical power. It can be interpolated from [39] that a 0.12 mm^2 PD will have a junction capacitance of approximately 10 pF. Thus, 10 pF PD input capacitance is chosen for 5 KHz BW cases.

On one hand, a 5 KHz BW is chosen because the majority of biomedical application in the literatures seek a similar BW value for PPG based sensors [39] and continuous wave NIRS receivers [40]. Despite that the actual frequency contents of the PPG signal lies between 0.5 Hz and 5 Hz [4], the duty cycle control of the transmitting LED, which serves to control the emitted power, is done at multiple KHz speed [41]. Thus, a TIA that has much higher BW than the frequency contents of the PPG is essential. However, attaining such a low BW (0.5 Hz to 5 Hz) in the succeeding stages is also necessary to reject the out of band noise and to achieve the required sensitivity. Some techniques are widely adopted to attain this low BW without sacrificing the chip area like MOS-Pseudo resistor [42], Miller capacitance multiplication [43], and α Block [44]. Those techniques are beyond the scope of this work.

On the other hand, the 100 MHz BW is chosen to assist the designers of higher BW biomedical applications like frequency domain NIRS (FD-NIRS) which utilizes 100 MHz BW or more with a relatively smaller PD capacitance [45]. A 1.5 pF PD is used in the FD-NIRS optical receiver presented in [46]. Thus, a 2 pF PD is considered reasonable for this application.

This paper is organized as follows, the transimpedance gain and noise mathematical models of each TIA topology are presented and discussed in the second section. The third section introduces the simulation results for the four mentioned cases with comparisons and discussions. The last section concludes the results and provides suggestions to the designer on what topology to use according to the target and device requirements.

II. TIAs Topologies

In this section, the transimpedance gain and the input referred noise current spectral density mathematical models are presented and discussed for all of the previously

mentioned TIAs topologies. The values of the resistances and MOSFETs' widths are tabulated for each simulation case at the end of each circuit subsection. Channel lengths of all MOSFETs are set to the minimum 120 nm length.

A. Common Source TIA (CS-TIA)

The CS-TIA is shown in Fig. 4. It uses a conventional CS voltage amplifier as the core amplifier with the shunt-shunt feedback to realize the current to voltage amplification. The topology is widely used since it is simple to design and occupies small chip area [47]–[49]. The transimpedance gain formula of the CS-TIA is described by:

$$Z(S)_{\text{TIA}} = \frac{R_{\text{out}} - |A_{\text{CS}}| R_F}{H(S^2) + H(S) + |A_{\text{CS}}| + 1} \quad (1a)$$

$$Z(0)_{\text{TIA}} \simeq -R_F \quad (1b)$$

$$H(S^2) = S^2 C_{\text{in}} C_{\text{out}} R_F R_{\text{out}} \quad (1c)$$

$$H(S) = S[(R_F + R_{\text{out}}) C_{\text{PD}} + R_{\text{out}} C_{\text{out}}] \quad (1d)$$

where R_{out} and A_{CS} are the open loop output resistance and the open loop gain of the CS amplifier respectively described by:

$$R_{\text{out}} = R_D // r_{\text{on}} \quad (2)$$

$$A_{\text{CS}} = -g_{\text{mn}} R_{\text{out}} \quad (3)$$

Using the feedback theory, the zero frequency input impedance is described by:

$$Z(0)_{\text{in}} = \frac{R_{\text{out}} + R_F}{|A_{\text{CS}}| + 1} \quad (4)$$

The total input capacitance including the miller effect is described by:

$$C_{\text{in}} = C_{\text{PD}} + (|A_{\text{CS}}| + 1) C_{\text{gdn}} \quad (5)$$

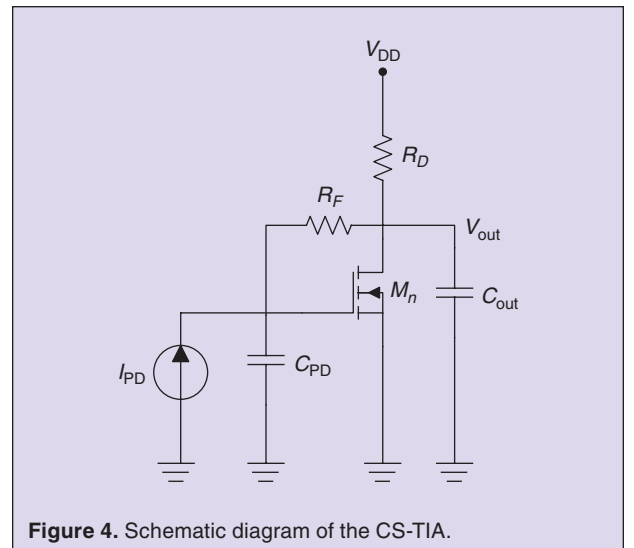


Figure 4. Schematic diagram of the CS-TIA.

where C_{PD} is the PD junction capacitance, C_{gdn} is the gate to drain capacitance of the NMOS transistor. Assuming that C_{in} is very large compared to C_{out} and it forms the dominant pole of the response, the BW can be approximated by:

$$BW \simeq \frac{1}{2\pi Z(0)_{in} C_{in}} = \frac{|A_{CS}| + 1}{2\pi (R_{out} + R_F) C_{in}} \quad (6)$$

It is clear from equations (4) and (6) that due to the feedback topology nature, the input impedance can be decreased with increasing the open loop gain which enhances the BW. However, increasing the open loop gain will result in a higher DC current consumption. Moreover, further increase in the open loop gain will increase the miller effect which at the end limits the BW enhancement. Therefore, a trade-off is manifested between the BW and the power consumption.

The total input referred noise current of the CS-TIA is described by:

$$\overline{I_{n,in}^2} = 4K_B T \left[\frac{g_{mn}^2 + (2\pi f C_{PD})^2}{(1 - g_{mn} R_F)^2} R_F + \frac{1 + (2\pi f C_{PD} R_F)^2}{(1 - g_{mn} R_F)^2} \left(\frac{1}{R_D} + g_{mn} \gamma \right) \right] \quad (7)$$

Table I. Simulation parameters of the CS-TIA.			
Case	W_{M_n}	R_D	R_F
5 KHz, Minimum Noise	8 μm	3 K Ω	11.5 M Ω
5 KHz, Minimum Power	1.56 μm	9 K Ω	10 M Ω
100 MHz, Minimum Noise	25 μm	1.5 K Ω	4.8 K Ω
100 MHz, Minimum Power	18 μm	9 K Ω	2.7 K Ω

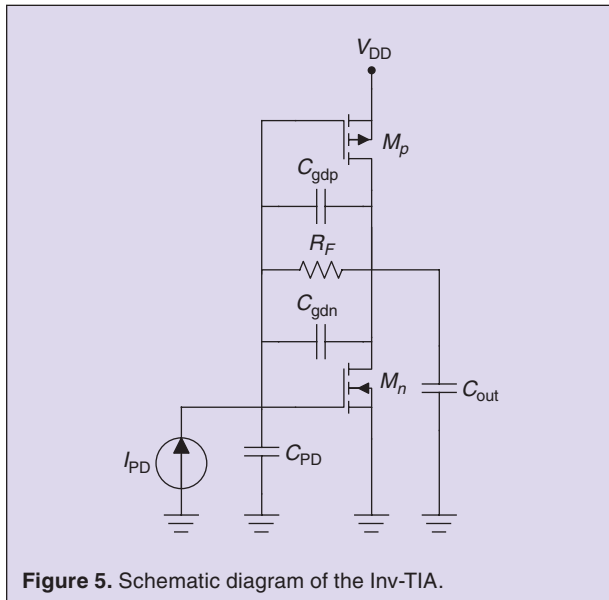


Figure 5. Schematic diagram of the Inv-TIA.

where K_B is the Boltzmann constant, T is the temperature in Kelvin, and γ is the MOSFET noise factor. The first term of equation (7) is the input noise contribution of R_F , the second term is the input noise due to M_n and R_D .

In addition, equation (7) reveals that the noise contribution of R_F dominates at low frequencies and the noise of M_n dominates at high frequencies. It is clear from equation (7) that there is a severe trade-off between the noise and g_{mn} , and so the power consumption. For example, as g_{mn} is reduced by shrinking the width of the transistor, the DC biasing current will decrease, however, the noise will be increased as well and vice versa. Moreover, it can be observed that at high frequencies, the noise of R_F is inversely proportional to its value which results in a lower total input noise at higher transimpedance gain. However, increasing R_F will also shrink the TIA's BW, see equation (6).

Furthermore, increasing R_D reduces the total input noise according to the second term of equation (7) and also enhances the open loop gain. However, the value of R_D cannot be increased beyond a certain limit to maintain a suitable voltage headroom and ensure NMOS saturation. The value of transistor sizing and resistances values for the four mentioned simulation cases are listed in table I.

B. Inverter TIA (Inv-TIA)

The schematic diagram of the Inv-TIA is shown in Fig. 5. It uses a CMOS inverter as a core amplifier (M_n , M_p) with a shunt-shunt feedback resistor (R_F) to realize the current to voltage amplification. CMOS inverter has been widely used as the core amplifier in many proposed high performance designs [50]–[54]. The Inv-TIA can provide a higher open loop gain and a higher gain bandwidth product (GBW) compared to the CS-TIA. This is due to the higher obtainable effective transconductance which is the sum of both NMOS and PMOS transconductances. Moreover, higher drain to source resistance provided by the active load M_p at the same DC voltage drop is achieved compared to the passive resistor in the CS-TIA. The transimpedance gain of the Inv-TIA is described by:

$$Z(S)_{TIA} = \frac{R_{out} - |A_{Inv}| R_F}{H(S^2) + H(S) + |A_{Inv}| + 1} \quad (8a)$$

$$Z(0)_{TIA} \simeq -R_F \quad (8b)$$

$$H(S^2) = S^2 C_{in} C_{out} R_F R_{out} \quad (8c)$$

$$H(S) = S[(R_F + R_{out}) C_{in} + R_{out} C_{out}] \quad (8d)$$

where A_{Inv} and R_{out} are the open loop gain and the open loop output resistance respectively which are described by:

$$A_{Inv} = -G_m R_{out} = -(g_{mn} + g_{mp}) R_{out} \quad (9)$$

$$R_{out} = r_{op} // r_{on} \quad (10)$$

where r_{on} and r_{op} are the drain-source resistances of M_n and M_p respectively, C_{in} is the total input capacitance consisted of the PD junction capacitance and the miller capacitance due to C_{gdn} and C_{gdp} described by:

$$C_{in} = C_{PD} + (C_{gdn} + C_{gdp})(|A_{Inv}| + 1) \quad (11)$$

Using the feedback theory, the zero frequency input impedance is described by:

$$Z(0)_{in} = \frac{R_{out} + R_F}{|A_{Inv}| + 1} \quad (12)$$

Assuming that C_{in} is very large compared to C_{out} so that the input pole is the dominant pole, the BW can then be approximated by:

$$BW \simeq \frac{1}{2\pi Z(0)_{in} C_{in}} = \frac{|A_{Inv}| + 1}{2\pi (R_{out} + R_F) C_{in}} \quad (13)$$

It is clear from equation (9) that the open loop gain of the Inv-TIA is higher than the open loop gain of the CS-TIA due to:

- 1) The higher effective transconductance (G_m).
- 2) The higher open loop output resistance that can be achieved at the same output DC voltage due to the active load M_p .

Accordingly, the Inv-TIA can achieve the same GBW at a lower power consumption compared to the CS-TIA.

The input referred noise current of the Inv-TIA is described by:

$$\overline{I_{n,in}^2} = 4K_B T \left[\frac{G_m^2 + (2\pi f C_{PD})^2}{(1 - G_m R_F)^2} R_F + \frac{1 + (2\pi f C_{PD} R_F)^2}{(1 - G_m R_F)^2} (g_{mn} \gamma_n + g_{mp} \gamma_p) \right] \quad (14)$$

where the first term is the noise of R_F and the second term is the noise contribution of M_n and M_p . Equation (14) reveals that R_F noise term dominates at low frequencies while the core amplifier's noise term dominates at higher frequencies. It should be denoted that the noise performance of the Inv-TIA is greater than that of the CS-TIA due to the increase of the transconductance G_m at the same DC biasing current. Similar to the CS-TIA, a trade-off between the DC biasing (power consumption) and the input referred noise is observed. The value of transistors widths and resistances values used in the simulation are listed in table II.

C. Inverter Cascode based TIA (InvCas-TIA)

The InvCas-TIA is shown in Fig. 6. It is an enhanced version of the Inv-TIA with a two introduced cascode transistors (M_{n2}, M_{p2}) which increase the open loop gain and enhance the GBW of the TIA. Also, the effect of the

miller capacitance introduced in the input is greatly reduced compared to both the CS-TIA and the Inv-TIA [29]. This is because the drains of the transistors M_{n1} and M_{p1} are connected to the source of the cascode transistors M_{n2} and M_{p2} . Thus, the resistances that are seen from the drains of M_{n1} and M_{p1} are almost equal to g_{mn2}^{-1} and g_{mp2}^{-1} respectively which are very small. Accordingly, the poles introduced due to the miller effect are shifted toward a higher frequency resulting in a greater BW compared to the CS-TIA and the Inv-TIA at the same transimpedance gain. The transimpedance gain of the InvCas-TIA is described by:

$$Z(S)_{TIA} = \frac{R_{out} - |A_{InvCas}| R_F}{H(S^2) + H(S) + |A_{InvCas}| + 1} \quad (15a)$$

$$Z(0)_{TIA} \simeq -R_F \quad (15b)$$

$$H(S^2) = S^2 C_{PD} C_{out} R_F R_{out} \quad (15c)$$

$$H(S) = S[(R_F + R_{out}) C_{PD} + R_{out} C_{out}] \quad (15d)$$

Table II.
Simulation parameters of the Inv-TIA.

Case	W_{M_n}	W_{M_p}	R_F
5 KHz, Minimum Noise	6 μm	7 μm	14.2 M Ω
5 KHz, Minimum Power	0.55 μm	1 μm	14.2 M Ω
100 MHz, Minimum Noise	18 μm	12 μm	9.5 K Ω
100 MHz, Minimum Power	3 μm	4 μm	4.6 K Ω

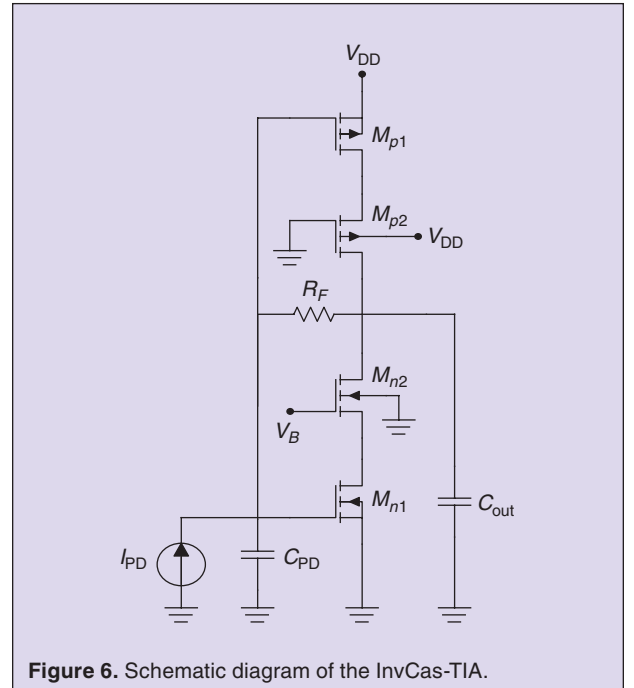


Figure 6. Schematic diagram of the InvCas-TIA.

where A_{InvCas} and R_{out} are the open loop gain and the open loop output resistance respectively described by:

$$R_{\text{out}} = \left(g_{mn2} + \frac{1}{r_{on1}} + \frac{1}{r_{on2}} \right) r_{on1} r_{on2} // \left(g_{mp2} + \frac{1}{r_{op1}} + \frac{1}{r_{op2}} \right) r_{op1} r_{op2} \quad (16)$$

$$A_{\text{InvCas}} = -G_m R_{\text{out}} = -(g_{mn1} + g_{mp1}) R_{\text{out}} \quad (17)$$

The zero frequency input resistance can be easily computed using the feedback theory and it is:

$$Z(0)_{\text{in}} = \frac{R_{\text{out}} + R_F}{|A_{\text{InvCas}}| + 1} \quad (18)$$

Assuming that C_{PD} is very large compared to C_{out} , the BW can be approximated by:

$$BW \simeq \frac{1}{2\pi Z(0)_{\text{in}} C_{\text{PD}}} = \frac{|A_{\text{InvCas}}| + 1}{2\pi (R_{\text{out}} + R_F) C_{\text{PD}}} \quad (19)$$

It is clear from equation (17) that the open loop gain has been greatly increased compared to the open loop gain of the Inv-TIA described in equation (9). Consequently, a higher BW and a higher GBW are obtained as illustrated by equation (19) compared to the Inv-TIA. Nevertheless, the InvCas-TIA has less voltage headroom per transistor which reduces the dynamic range and deteriorate the linearity compared to the Inv-TIA. Those observations are confirmed by the later simulation results.

The input noise current of the InvCas-TIA is given by:

$$\begin{aligned} \overline{I_{n,\text{in}}^2} = & 4K_B T \left[\frac{G_m^2 + (2\pi f C_{\text{PD}})^2}{(1 - G_m R_F)^2} R_F \right. \\ & + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{(1 - G_m R_F)^2} (g_{mn1} \gamma_n + g_{mp1} \gamma_p) \\ & + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{\left((1 - G_m R_F) \left(g_{mn2} + \frac{1}{r_{on2}} \right) r_{on1} \right)^2} g_{mn2} \gamma_n \\ & \left. + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{\left((1 - G_m R_F) \left(g_{mp2} + \frac{1}{r_{op2}} \right) r_{op1} \right)^2} g_{mp2} \gamma_p \right] \quad (20) \end{aligned}$$

Equation (20) is consisted of four terms, the first term describes the input noise contribution due to R_F , the second term is the input referred noise due to M_{n1} and M_{p1} . The third and fourth terms are the contribution of M_{n2} and M_{p2} respectively.

It can be deduced that the noise contribution of R_F dominates at low frequencies while the cascode transistors dominate at higher frequencies. Furthermore, due to the extra two noise term of the cascode transistor in equation (20), the noise performance is degraded at high operating frequencies compared to the Inv-TIA. However, because of the higher transimpedance gain of the InvCas-TIA that is obtained at the same BW (higher R_F), the low frequency input noise is reduced compared to the Inv-TIA. This makes the topology very appealing for the high sensitivity biomedical applications. The value of transistor widths and resistances that are used for this study are listed in table III.

D. Regulated Inverter based Cascode TIA (RIC-TIA)

The schematic diagram of the RIC-TIA is shown in Fig. 7. The advantage of the RIC-TIA compared to the InvCas-TIA is the regulation of M_{n2} and M_{p2} . Accordingly, the transconductance of M_{p2} and M_{n2} are multiplied by the gains of Amp.1 and Amp.2 respectively as shown in the following mathematical model. Also, biasing the cascode transistors is achieved without the need of

Table III. Simulation parameters of the INVCAS-TIA.					
Case	$W_{M_{n1}}$	$W_{M_{n2}}$	$W_{M_{p1}}$	$W_{M_{p2}}$	R_F
5 KHz, Minimum Noise	13 μm	7 μm	8.1 μm	5 μm	16 M Ω
5 KHz, Minimum Power	0.6 μm	3.5 μm	0.55 μm	2.5 μm	16.8 M Ω
100 MHz, Minimum Noise	13 μm	28 μm	22 μm	15 μm	61 K Ω
100 MHz, Minimum Power	2.5 μm	5 μm	4 μm	2.6 μm	8 K Ω

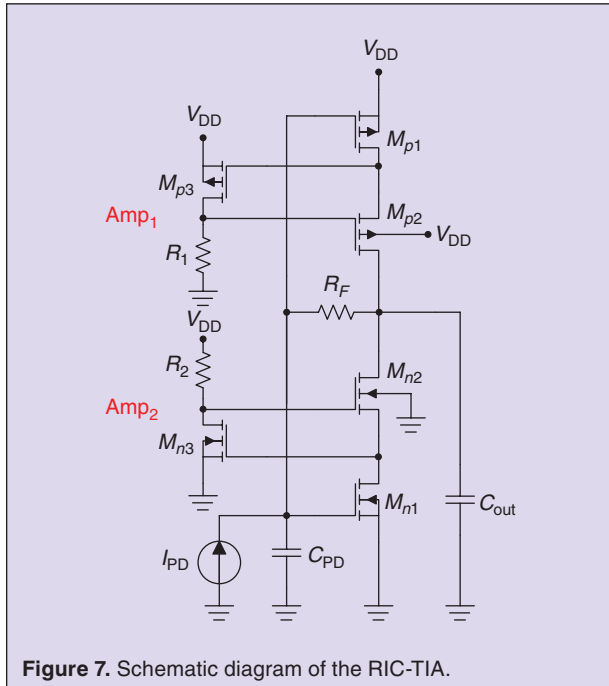


Figure 7. Schematic diagram of the RIC-TIA.

additional biasing circuitry. The transimpedance gain of the RIC-TIA is described by:

$$Z(S)_{\text{TIA}} = \frac{R_{\text{out}} - |A_{\text{RIC}}|R_F}{H(S^2) + H(S) + |A_{\text{RIC}}| + 1} \quad (21a)$$

$$Z_{\text{TIA}}(0) \simeq -R_F \quad (21b)$$

$$H(S^2) = S^2 C_{\text{PD}} C_{\text{out}} R_F R_{\text{out}} \quad (21c)$$

$$H(S) = S[(R_F + R_{\text{out}})C_{\text{PD}} + R_{\text{out}}C_{\text{out}}] \quad (21d)$$

where A_{RIC} and R_{out} are the open loop gain and the open loop output resistance of the voltage amplifier respectively given by:

$$A_{\text{RIC}} = -G_m R_{\text{out}} = -(g_{\text{mn1}} + g_{\text{mp1}})R_{\text{out}} \quad (22)$$

$$R_{\text{out}} = \left(g_{\text{mn2}}(|A_2| + 1) + \frac{1}{r_{\text{on1}}} + \frac{1}{r_{\text{on2}}} \right) r_{\text{on1}} r_{\text{on2}} \\ // \left(g_{\text{mp2}}(|A_1| + 1) + \frac{1}{r_{\text{op1}}} + \frac{1}{r_{\text{op2}}} \right) r_{\text{op1}} r_{\text{op2}} \quad (23)$$

where $G_m = g_{\text{mn1}} + g_{\text{mp1}}$ is the transconductance of the open loop inverter cascode voltage amplifier, R_F is the shunt-shunt feedback resistor, C_{PD} is the photodiode junction capacitance, A_1 , and A_2 are the gains of the regulating amplifier Amp1. and Amp2. respectively which are described by:

$$A_1 = -g_{\text{mp3}}(R_1 // r_{\text{op3}}) \quad (24a)$$

$$A_2 = -g_{\text{mn3}}(R_2 // r_{\text{on3}}) \quad (24b)$$

Using the feedback theory, the input impedance is obtained and it is described by:

$$Z_{\text{in}}(0) = \frac{R_{\text{out}} + R_F}{|A_{\text{RIC}}| + 1} \quad (25)$$

The BW can be approximated by:

$$BW \simeq \frac{1}{2\pi Z_{\text{in}}(0) C_{\text{PD}}} = \frac{|A_{\text{RIC}}| + 1}{2\pi (R_{\text{out}} + R_F) C_{\text{PD}}} \quad (26)$$

It is clear from equation (23) that the transconductance of M_{n2} and M_{p2} are multiplied by the factors $(A_1 + 1)$ and $(A_2 + 1)$ respectively. Accordingly, an increase in the open loop output resistance and the open loop gain are obtained. Therefore, the input impedance is reduced and higher transimpedance gain is achievable at the same BW compared to the InvCas-TIA. Looking from another perspective, the RIC-TIA provides the same open loop gain and the same GBW at a smaller g_{mn1} and g_{mp1} compared to the InvCas-TIA. Consequently, lower DC biasing current and power consumption are achievable for the same GBW compared to the InvCas-TIA.

Input referred noise current of the RIC-TIA is presented by:

$$\overline{I_{n,\text{in}}^2} = 4K_B T \left[\frac{(G_m)^2 + (2\pi f C_{\text{PD}})^2}{(1 - G_m R_F)^2} R_F \right. \\ + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{(1 - G_m R_F)^2} (g_{\text{mn1}} \gamma_n + g_{\text{mp1}} \gamma_p) \\ + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{\left((1 - G_m R_F) \left(g_{\text{mn2}}(|A_2| + 1) + \frac{1}{r_{\text{on2}}} \right) r_{\text{on1}} \right)^2} g_{\text{mn2}}^2 \gamma_n \\ + \frac{1 + (2\pi f C_{\text{PD}} R_F)^2}{\left((1 - G_m R_F) \left(g_{\text{mp2}}(|A_1| + 1) + \frac{1}{r_{\text{op2}}} \right) r_{\text{op1}} \right)^2} g_{\text{mp2}}^2 \gamma_p \\ + \frac{(r_{\text{op3}} // R_1)^2 g_{\text{mp2}}^2 r_{\text{op2}}^2 (1 + (2\pi f C_{\text{PD}} R_F)^2)}{(1 - G_m R_F)^2 R_{\text{out}}^2} B_1 \\ \left. + \frac{(r_{\text{on3}} / R_2)^2 g_{\text{mn2}}^2 r_{\text{on2}}^2 (1 + (2\pi f C_{\text{PD}} R_F)^2)}{(1 - G_m R_F)^2 R_{\text{out}}^2} B_2 \right] \quad (27a)$$

$$B_1 = \left(g_{\text{mp3}} \gamma_n + \frac{1}{R_1} \right) \quad (27b)$$

$$B_2 = \left(g_{\text{mn3}} \gamma_n + \frac{1}{R_2} \right) \quad (27c)$$

where the first term is the input referred noise current contribution of R_F . The second term is the input referred noise due to M_{n1} and M_{p1} . The third and fourth terms are due to the cascode transistors M_{n2} and M_{p2} respectively. The fifth and the sixth terms are the noise contribution of Amp1. and Amp2. respectively. Since R_{out} is very large, the noise contribution due to the regulating amplifier is sufficiently small compared to the noise contribution of M_{n1} , M_{p1} and R_F .

Also, due to the regulation of the cascode transistors, their transconductance (g_{mn2} and g_{mp2}) are multiplied by $(|A_2| + 1)$ and $(|A_1| + 1)$ respectively which decreases the noise contribution of the cascode transistors. Consequently, the noise increase due to the added regulating amplifiers is expected to be compensated by the enhancement of the effective transconductance. Simulation parameters are listed in table IV.

Table IV.
Simulation parameters of the RIC-TIA.

	5 KHz, Min Noise	5 KHz, Min Power	100 MHz, Min Noise	100 MHz, Min Power
W_{Mn1}	10 μm	4.5 μm	8.5 μm	2.5 μm
W_{Mn2}	10 μm	4.5 μm	23 μm	2.5 μm
W_{Mp1}	7.5 μm	0.6 μm	22 μm	2.6 μm
W_{Mp2}	10 μm	0.6 μm	12 μm	2.2 μm
R_F	18 M Ω	18 M Ω	66 K Ω	10 K Ω
W_{Mp3}	2 μm	2 μm	1 μm	1 μm
W_{Mn3}	5 μm	5 μm	1 μm	1 μm
R_1	100 K Ω	100 K Ω	9 K Ω	9 K Ω
R_2	300 K Ω	300 K Ω	9 K Ω	9 K Ω

E. Common Gate TIA (CG-TIA)

The circuit of the CG-TIA is shown in Fig. 8. The CG-TIA is used due to its relatively low power consumption and low input impedance [55]–[57]. The input photocurrent is fed to the source of the common gate transistor M_n and the output is taken from its drain. The CG-TIA provides a low input impedance $\simeq g_{mn}^{-1}$ which serves to achieve a relatively high BW. The transimpedance gain of the CG-TIA is described by:

$$Z(S)_{TIA} = \frac{(g_{mn}r_{on} + 1)R_D}{(SC_{out}R_D + 1)(SC_{PD}(R_D + r_{on}) + g_{mn}r_{on} + 1)} \quad (28a)$$

$$Z(0)_{TIA} = R_D \quad (28b)$$

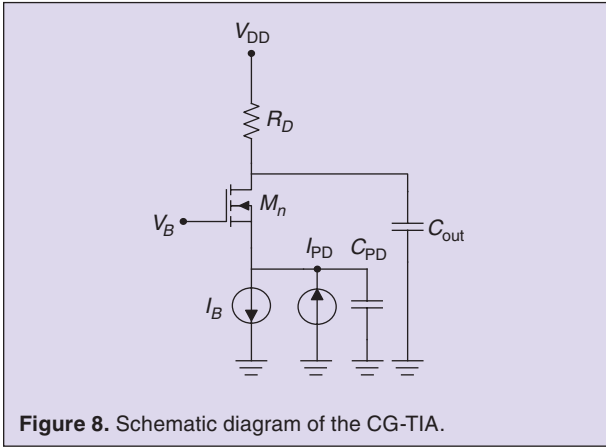
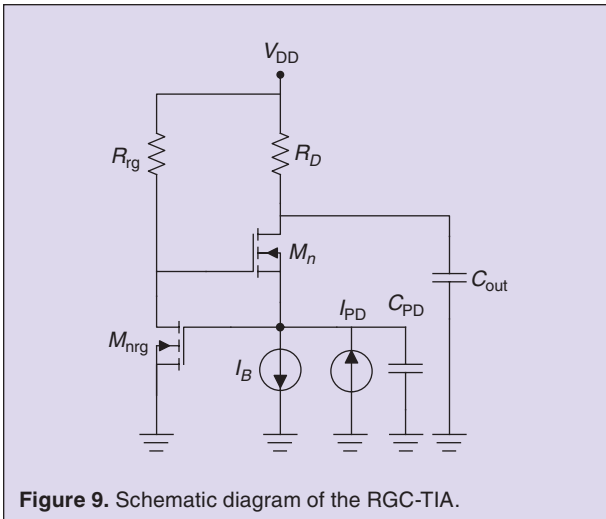


Table V.
Simulation parameters of the CG-TIA.

Case	W_{M_n}	R_D
5 KHz	2 μm	12.5 M Ω
100 MHz	30 μm	4.5 K Ω



where g_{mn} is the transconductance of M_n . The zero frequency input resistance is given by:

$$Z(0)_{in} = \frac{R_D + r_{on}}{g_{mn}r_{on} + 1} \simeq \frac{1}{g_{mn}} \quad (29)$$

Assuming that the dominant pole is resulted from C_{PD} and $Z(0)_{in}$, thus, the BW is described by:

$$BW = \frac{g_{mn}r_{on} + 1}{2\pi C_{PD}(R_D + r_{on})} \simeq \frac{g_{mn}}{2\pi C_{PD}} \quad (30)$$

Consequently, obtaining large BW means increasing the transconductance g_{mn} and hence the DC current consumption of M_n . Accordingly, equation (30) shows a tradeoff between the BW and the power consumption for the CG-TIA.

The input referred noise current of the CG-TIA is presented by:

$$\overline{I_{n,in}^2} = 4K_B T \left[\frac{(2\pi f C_{in} r_{on})^2 + (g_{mn} r_{on})^2 + 1}{(1 + g_{mn} r_{on})^2} R_D + \frac{(2\pi f C_{in} r_{on})^2}{(1 + g_{mn} r_{on})^2} g_{mn} \gamma_n + g_{mnB} \gamma_n \right] \quad (31)$$

where g_{mnB} is the transconductance of the biasing current source transistor. The first term in equation (31) is the noise contribution of R_D , the second and third terms are the input noise caused by M_n and the biasing current source transistor respectively. One of the major drawbacks of the CG-TIA is that the noise of the biasing current source is directly referred to the input. Therefore, the total input noise is relatively high compared to its closed loop counterpart. It can be concluded from equation (31) that the second low frequency dominant noise source is R_D . Also, equation (31) shows that the noise of M_n approaches the noise of R_D at higher frequencies. Furthermore, since the dominant noise term of the biasing current source increases with g_{mnB} , the trade-off between the noise and power consumption is no longer presented. Simulation parameters of the CG-TIA are listed in table V.

F. Regulated Cascode TIA (RGC-TIA)

The circuit of the RGC-TIA is shown in Fig. 9. It is an enhanced version of the CG-TIA. The key idea is that the gate of M_n is regulated by a common source voltage amplifier (M_{nrg} , R_{nrg}). This regulation is achieved by connecting the source of M_n to the input of the regulating amplifier and connecting the output of the regulating amplifier to the gate of M_n . Accordingly, the regulation boosts the transconductance of M_n by a multiplication factor equals to the gain of this regulating amplifier. Therefore, the input impedance is decreased and the BW is extended compared to the CG-TIA.

Thanks to the topology's low input impedance, the RGC-TIA is used very efficiently to isolate the large area PD

capacitance from the circuit [58]. Therefore, the RGC-TIA is widely used in many literatures because of its low input impedance that is achievable at a relatively low power consumption [59]–[65]. By analyzing the small signal model, the transimpedance gain is obtained and it is given by:

$$Z(S)_{\text{TIA}} = \frac{(G_m r_{\text{on}} + 1) R_D}{(SC_{\text{out}} R_D + 1)(SC_{\text{PD}}(R_D + r_{\text{on}}) + G_m r_{\text{on}} + 1)} \quad (32a)$$

$$Z(0)_{\text{TIA}} = R_D \quad (32b)$$

where G_m is the effective transconductance of the cascode stage described by:

$$G_m = g_{\text{mn}}(|A_{\text{rg}}| + 1) \quad (33)$$

where A_{rg} is the voltage gain of the regulating amplifier which is presented by:

$$A_{\text{rg}} = -g_{\text{mnr}}(r_{\text{onrg}}//R_{\text{rg}}) \quad (34)$$

The zero frequency input resistance is given by:

$$Z(0)_{\text{in}} = \frac{R_D + r_{\text{on}}}{G_{\text{mn}} r_{\text{on}} + 1} \simeq \frac{1}{G_{\text{mn}}} \quad (35)$$

Assuming that the dominant pole is resulted from C_{PD} and $Z(0)_{\text{in}}$, then the BW is described by:

$$BW = \frac{G_{\text{mn}} r_{\text{on}} + 1}{2\pi C_{\text{PD}}(R_D + r_{\text{on}})} \simeq \frac{G_{\text{mn}}}{2\pi C_{\text{PD}}} \quad (36)$$

Equation (33) clearly shows an $(|A_{\text{rg}}| + 1)$ enhancement of the transconductance compared to the CG-TIA. Therefore, the BW is increased at the same transimpedance gain and a higher GBW can be obtained.

The total input referred noise current of the RGC-TIA is demonstrated by equation (37) where g_{mnB} is the transconductance of the biasing current source transistor, R_D and M_n noise contribution is described by the first and second term respectively. The third term is the noise contribution of the biasing current source NMOS, the fourth term is the noise contribution of the regulating amplifier.

Equation (37) also reveals that the noise of the biasing current source transistor is directly referred to the input. Accordingly, the total integrated input noise current of the RGC-TIA is expected to be higher compared to its closed loop topologies counterparts. However, since the transconductance is higher by a factor $(|A_{\text{rg}}| + 1)$, the noise performance of the RGC-TIA is expected to be better than the CG-TIA at low frequencies.

$$\begin{aligned} \overline{I_{n,\text{in}}^2} = 4K_B T \left[\frac{(2\pi f C_{\text{in}} r_{\text{on}})^2 + (G_m r_{\text{on}})^2 + 1}{(1 + G_m r_{\text{on}})^2} R_D \right. \\ + \frac{(2\pi f C_{\text{in}} r_{\text{on}})^2}{(1 + G_m r_{\text{on}})^2} g_m \gamma_n + g_{\text{mnB}} \gamma_n \\ \left. + \frac{(2\pi f C_{\text{PD}} g_{\text{mn}} r_{\text{on}} (R_{\text{rg}}//r_{\text{onrg}}))^2}{(1 + G_m r_{\text{on}})^2} \left(g_{\text{mnr}} \gamma_n + \frac{1}{R_{\text{rg}}} \right) \right] \quad (37) \end{aligned}$$

It should be clarified that to obtain a high transimpedance gain and 5 KHz BW, the value of R_D must be increased to an order of multiple MOhms. Consequently, the biasing current source I_B must be less than 100 nA to allow reasonable voltage headroom which forces the NMOS to work in the subthreshold region. Thus, open loop topologies like CG-TIA and RGC-TIA are preferred in high BW designs like FD-NIRS and time domain near infrared spectroscopy (TD-NIRS) and are rarely used in low BW applications (PPG sensors). Also, the trade-off between the noise and the power consumption is not presented, as the same as in the case of the CG-TIA. Simulation parameters used for simulating the RGC-TIA are listed in table VI.

G. Current Reuse TIA (CR-TIA)

The schematic diagram of the CR-TIA is shown in Fig. 10. The topology is consisted of a common source amplifier with a shunt-shunt feedback (M_{n1} , R_F) forming a CS-TIA. The CS-TIA is followed by a common gate stage (M_{n2} , M_p). First, the input current is fed to the CS-TIA, then, the output voltage of the CS-TIA is fed to the common gate stage for further amplification. Therefore, the input is amplified two times using the same DC biasing current which reduces the power consumption (current reuse). Nevertheless, smaller voltage headroom is attained per transistor which degrades the linearity compared to the CS-TIA.

Table VI.
Simulation parameters of the RGC-TIA.

Case	W_{M_n}	R_D	R_{rg}	$W_{M_{\text{nr}}}$
5 KHz	10 μm	16.2 M Ω	80 K Ω	1 μm
100 MHz	30 μm	19 K Ω	5 K Ω	5 μm

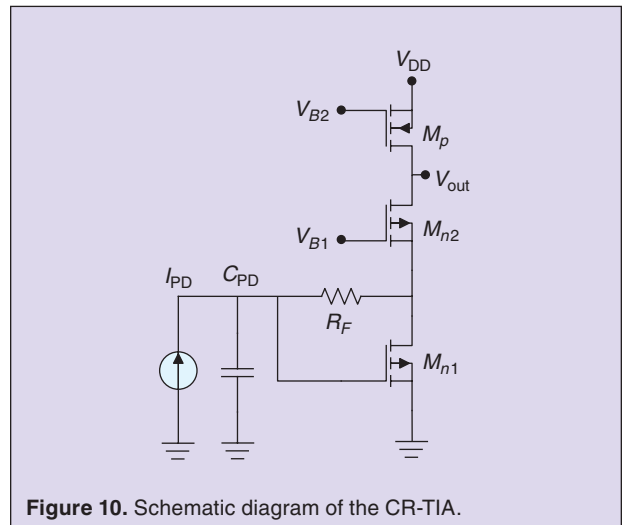


Figure 10. Schematic diagram of the CR-TIA.

Using the small signal model of the CR-TIA, the transimpedance gain is deduced and is described by: [33]

$$Z(S)_{TIA} = \frac{(R_{CS} - |A_{CS}|R_F)A_{CG}}{SC_{PD}(R_F + R_{CS}) + |A_{CS}| + 1} \quad (38a)$$

$$Z(0)_{TIA} \simeq -R_F A_{CG} \quad (38b)$$

where R_{CS} is the total resistance seen by the drain of M_{n1} , A_{CS} and A_{CG} are the open loop gains of the common source and the common gate stages respectively which are given by:

$$A_{CS} = -g_{mn1}R_{CS} \quad (39a)$$

$$R_{CS} = \frac{1}{g_{mn2}} // r_{on1} // r_{on2} \quad (39b)$$

$$A_{CG} = g_{mn2}(r_{op} // r_{on2}) \quad (40)$$

The zero frequency input impedance is described by:

$$Z(0)_{in} = \frac{R_{CS} + R_F}{|A_{CS}| + 1} \quad (41)$$

assuming that $(C_{PD}, Z(0)_{in})$ forms the dominant pole of the circuit, then the BW is expressed by:

Table VII. Simulation parameters of the CR-TIA.				
Case	$W_{M_{n1}}$	$W_{M_{n2}}$	W_{M_p}	R_F
5 KHz Minimum Noise	60 μm	12 μm	6 μm	9 M Ω
5 KHz Minimum Power	1 μm	12 μm	1 μm	6.6 M Ω
100 MHz Minimum Noise	33 μm	10 μm	33 μm	5.4 K Ω
100 MHz Minimum Power	11 μm	3.7 μm	11 μm	4 K Ω

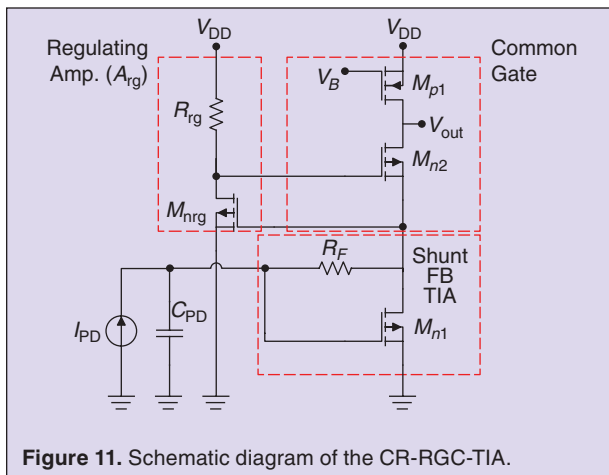


Figure 11. Schematic diagram of the CR-RGC-TIA.

$$BW \simeq \frac{1}{2\pi Z(0)_{in} C_{PD}} = \frac{|A_{CS}| + 1}{2\pi C_{PD}(R_{CS} + R_F)} \quad (42)$$

Equation (38 b) shows that the input signal is amplified two times, one time using the CS-TIA ($-R_F$) and the other time with the common gate stage (A_{CG}). Accordingly, higher transimpedance gain can be obtained at almost the same BW compared to the CS-TIA. Also, the effect of the miller capacitance due to $C_{gd,mn1}$ is greatly reduced since the source of M_{mn2} provides a low resistance node approximated by $1/g_{mn2}$. Viewed from another perspective, CR-TIA can achieve the same transimpedance gain as the CS-TIA at a relatively lower power consumption. However, due to the high attainable transimpedance gain, the maximum overloading input current is limited resulting in a lower dynamic range compared to CS-TIA.

The noise equivalent circuit of the CR-TIA is used to deduce the total input referred noise current described by equation (43). The first term of equation (43) is the noise contribution of M_{n2} (first two lines), the second term is the noise generated by R_F . The third term is the noise contribution of M_{n1} and the forth term is due to M_p . Careful inspection of equation (43) reveals that R_F noise dominates at low frequencies while the cascode transistor M_{n2} noise dominates at higher frequencies.

It is clear that the noise of the CR-TIA is higher than the CS-TIA because of the extra noise sources generated by M_{n2} and M_p . In addition, the gain is determined not only by R_F but also by A_{CG} . Thus, the value of R_F in the CR-TIA is much lower than in CS-TIA for the same transimpedance gain. Accordingly, the noise generated by R_F in the CR-TIA is greater than in CS-TIA which deteriorates the noise of the CR-TIA even further. This observation is clear in the upcoming simulation results. Simulation parameters used in the four cases are listed in table VII.

$$\begin{aligned} \overline{I_{n,in}^2} = 4K_B T \left[\left(\frac{(2\pi f C_{PD} R_F)^2 + 1}{(g_{mn1} R_F - 1)^2} \right) \left(\left(\frac{1}{g_{mn2} + \frac{1}{r_{on2}}} \right) R_{CS} - 1 \right)^2 \right. \\ + \left(\frac{1}{A_{CG} + 1} \left(\frac{1}{(1 - g_{mn1} R_F)} + \frac{r_{on2}}{R_F} \right) \right)^2 g_{mn2} \gamma_n \\ + \left(\frac{(2\pi f C_{PD})^2 + g_{mn1}^2}{(g_{mn1} R_F - 1)^2} \right) R_F + \frac{(2\pi f C_{PD} R_F)^2 + 1}{(g_{mn1} R_F - 1)^2} g_{mn1} \gamma_n \\ \left. + \left[\left(\left(\frac{1}{g_{mn2} + \frac{1}{r_{on2}}} \right) A_{CS} \right)^2 + \left(\frac{1 + A_{CS}}{\left(g_{mn2} + \frac{1}{r_{on2}} \right) A_{CS} R_F} \right)^2 \right] g_{mp} \gamma_p \right] \quad (43) \end{aligned}$$

H. Current Reuse with RGC TIA (CR-RGC-TIA)

The CR-RGC-TIA is shown in Fig. 11 [34]. It is a modified version of the CR-TIA topology shown in Fig. 10. The enhancement of this topology over the CR-TIA is the regulating amplifier A_{rg} which regulates M_{n2} . This regulation increases the effective transconductance of the

transistor M_{n2} by a factor equals to the gain of the amplifier A_{rg} and enhances the GBW of the TIA. This comes at the cost of the noise and power consumption increase due to the added regulating amplifier.

The transimpedance gain of the CR-RGC-TIA is described by:

$$Z_{TIA}(S) = \frac{(R_{CS} - A_{CS}R_F)A_{RGC}}{SC_{PD}(R_{CS} + R_F) + A_{CS} + 1} \quad (44a)$$

$$Z_{TIA}(0) \simeq -R_F A_{RGC} \quad (44b)$$

where C_{PD} is the photodiode junction capacitance, R_{CS} is the resistance seen by the drain of M_{n1} which is described by:

$$R_{CS} = r_{on1} // r_{on2} // \frac{1}{G_{mn2}} \quad (45)$$

G_{mn2} is the effective transconductance of M_{n2} given by:

$$G_{mn2} = g_{mn2}|A_{rg}| = g_{mn2}g_{mnrg}(R_{rg} // r_{onrg}) \quad (46)$$

where A_{rg} is the gain of the regulating amplifier, A_{CS} and R_{RGC} are the gain of the open loop common source amplifier and the gain of the regulated cascode respectively which are given by:

$$A_{CS} = -g_{mn1}R_{CS} \quad (47)$$

$$A_{RGC} = G_{mn2}(r_{op1} // r_{on2}) \quad (48)$$

Using the feedback theory the input resistance of the TIA at zero frequency is described by:

$$Z(0)_{in} = \frac{R_{CS} + R_F}{|A_{CS}| + 1} \quad (49)$$

Hence, the BW can be approximated by:

$$BW \simeq \frac{1}{2\pi Z_{in}(0)C_{PD}} = \frac{|A_{CS}| + 1}{2\pi(R_{CS} + R_F)C_{PD}} \quad (50)$$

Equation (46) shows that the transconductance of the transistor M_{n2} is increased by an $|A_{rg}|$ factor compared to the ordinary CR-TIA. Therefore, the gain can be increased at the same BW and a higher GBW is obtained according to equations (44b) and (48). However, CR-RGC-TIA would experience more power consumption due to the added regulating amplifier. Also, since the topology achieves higher transimpedance gain than CR-TIA, the dynamic range is expected to be less which is confirmed by the simulation results.

The total input referred noise current of the CR-RGC-TIA is described by equation (51a) in which the first term is produced by M_{n2} . The second term is due to the noise contribution of R_F and the third term is the noise contribution of M_{n1} . The fourth term is resulted from M_{p1} while the fifth term is the noise contribution of M_{nrg} and R_{rg} . Compared to the CR-TIA, the CR-RGC-TIA exhibits higher input referred noise current because of the extra noise sources of the regulating amplifier. Furthermore, since CR-RGC-TIA can achieve higher transimpedance gain but with larger input noise, its dynamic range is expected to be less than CR-TIA. Simulation parameter used for CR-RGC-TIA are listed in table VIII.

$$\begin{aligned} \overline{I_{n,in}^2} = 4K_B T \left[\left(\frac{(2\pi f C_{PD} R_F)^2 + 1}{(g_{mn1} R_F - 1)^2} \left(\frac{1}{Dx R_{CS}} - 1 \right)^2 \right. \right. \\ \left. \left. + \left(\frac{1}{A_{RGC} + 1} \left(\frac{1}{(1 - g_{mn1} R_F)} + \frac{r_{on2}}{R_F} \right) \right)^2 \right] g_{mn2} \gamma_n \right. \\ \left. + \frac{(2\pi f C_{PD})^2 + g_{mn1}^2 R_F^2}{(g_{mn1} R_F - 1)^2} R_F + \frac{(2\pi f C_{PD} R_F)^2 + 1}{(g_{mn1} R_F - 1)^2} g_{mn1} \gamma_n \right. \\ \left. + \left[\frac{(2\pi f C_{PD} R_F)^2 + (A_{CS} + 1)^2}{(Dx A_{CS} R_F)^2} \right] g_{mp} \gamma_{p1} \right. \\ \left. + \frac{(r_{onrg} // R_{rg})^2 g_{mn2}^2 r_{on2}^2 (1 + (2\pi f C_{PD} R_F)^2)}{(1 - g_{m1} R_F)^2 R_{CS}^2} W \right] \quad (51a) \end{aligned}$$

$$Dx = g_{mn2}|A_{rg}| + \frac{1}{r_{on2}} \quad (51b)$$

$$W = \left(g_{mnrg} \gamma_n + \frac{1}{R_{rg}} \right) \quad (51c)$$

III. Simulation Results and Comparisons

In this section, the simulation results obtained at the previously mentioned four cases are introduced for all of the investigated topologies. Comparisons between those simulation results in all cases are listed and discussed. Both Figure of Merits (FoM₁) and (FoM₂) [58] are used to compare the investigated topologies where:

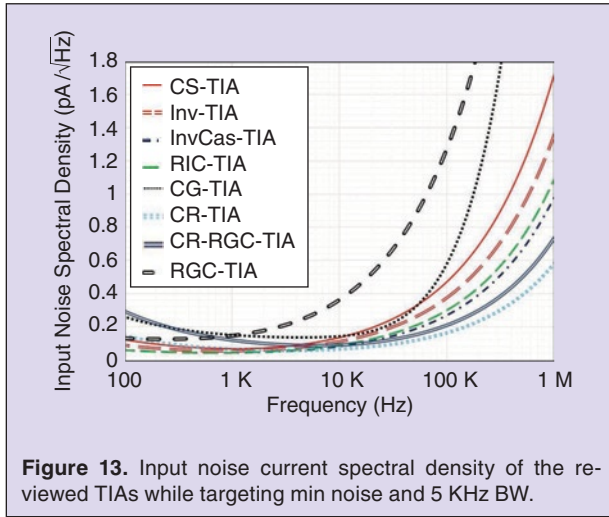
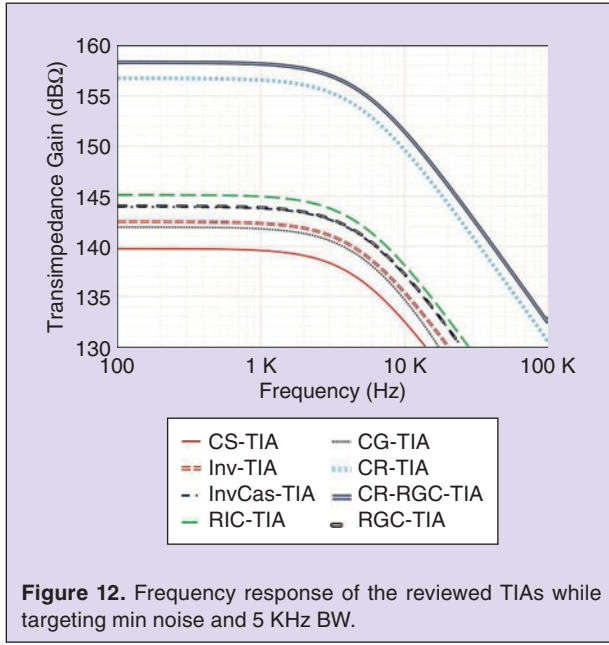
$$FoM_1 = \frac{\text{Gain} \cdot BW \cdot C_{in}}{I_{noise} \cdot \text{Power}} \quad (52a)$$

$$FoM_2 = FoM_1 I_{p-p}^{Ovl} \quad (52b)$$

where I_{noise} is the total integrated input referred noise current, I_{p-p}^{Ovl} is the maximum overloading sinusoidal

Table VIII.
Simulation parameters of the CR-RGC-TIA.

Case	$W_{M_{n1}}$	$W_{M_{n2}}$	$W_{M_{p1}}$	R_F	$W_{M_{nrg}}$	R_{rg}
5 KHz Minimum Noise	32 μm	12 μm	5.2 μm	5 M Ω	5 μm	4.2 K Ω
5 KHz Minimum Power	2.5 μm	12 μm	1.2 μm	4.7 M Ω	1 μm	10 K Ω
100 MHz Minimum Noise	38 μm	30 μm	15 μm	6 K Ω	1 μm	6 K Ω
100 MHz Minimum Power	12 μm	7 μm	4 μm	3.8 K Ω	1 μm	6 K Ω



input photocurrent which is the input current that causes 1% total harmonic distortion (THD) at the output [[66]]. The THD is computed according to:

$$\text{THD}\% = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1} \times 100 \quad (53)$$

where V_1 is the voltage of the fundamental frequency component, V_2 , V_3 , V_4 are the second, third, and forth harmonics. A 50 Hz sin wave is used for the 5 KHz BW cases and 1 MHz sine wave is used for 100 MHz BW to compute the THD %. The dynamic range is also listed in the comparison table and it is described by:

$$\text{DR} = 20 \text{ Log } \frac{I_{p-p}^{\text{Ovl}}}{I_{\text{noise}}} \quad (54)$$

It worth denoting that for minimum noise case, the power would increase when the noise is minimized. However, to allow reasonable comparison background, a maximum, equal power value is set for all topologies. Thus, the studied design noise performance can be exposed at the same power consumption. The same procedure is adopted for the maximum noise limit when minimizing the power consumption, thus, the studied topologies power consumption are compared at the same input referred noise current. Furthermore, the FoM_1 described by equation (52) is divided by 1000 in the 5 KHz BW cases for readability.

A. Case 1: $C_{PD} = 10 \text{ pF}$, 5 KHz BW, Minimum Noise

The frequency response and the input referred noise current spectral density of the reviewed TIAs are shown in Figs. 12 and 13 respectively. Also, a summary of the obtained simulation results for the minimum noise and 5 KHz BW case is listed in table IX.

Comparing the CS, Inv, InvCas, and RIC-TIA, the RIC-TIA is able to achieve the highest open loop gain due to

Table IX. A comparison between the reviewed TIA topologies at $C_{PD} = 10 \text{ pF}$ and 5 KHz BW while targeting minimum noise.								
Topology	Gain (dBΩ)	BW (kHz)	Total Integrated Input Noise pA_{rms}	Power μW	I_{p-p}^{Ovl} nA _{p-p}	DR (dB)	FoM1	FoM2
CS-TIA	139.6	5	5.9	272	77	82.3	297.5	22910.8
Inv-TIA	142.3	5	4.7	272	67	83.1	509.7	34149
InvCas-TIA	143.8	5	3.6	272	44	81.7	790.9	34798
RIC-TIA	145.1	5	3.75	272	41	80.8	882	36154
CR-TIA	156.7	5	4.9	272	2.4	53.8	2565.7	6157.7
CR-RGC-TIA	158.3	5	8.6	272	1.2	42.9	1757.5	2109
CG-TIA	141.5	5	10.56	0.044	0.67	36	1279×10^3	857×10^3
RGC-TIA	144	5	14.3	6.8	0.53	31.4	8149.4	4319.2

its high effective transconductance for the input transistors. Consequently, it attains the highest transimpedance gain of the four topologies. Also, due to the high effective transconductance of the RIC-TIA core amplifier, it has the second lowest input referred noise at the same power consumption and scores the highest FoM_1 of the four topologies. Accordingly, the RIC-TIA is very suitable for small input current and high sensitivity applications.

The simulation results also confirm that higher open loop gain topologies obtain higher performance. For example, InvCas-TIA outperforms Inv-TIA and CS-TIA in terms of GBW and input referred noise because of its superior open loop gain at the same power consumption. Moreover, the higher the open loop gain of the core amplifier the lower the total input referred noise. Despite that higher gain means lower I_{p-p}^{Ovl} , InvCas-TIA and RIC-TIA also achieve competitive DR and score the highest FoM_2 thanks to their low input referred noise current which compensates the I_{p-p}^{Ovl} reduction. When it comes to only the DR, the Inv-TIA and the CS-TIA shows the superiority.

Studying the results of the CR-TIA and the CR-RGC-TIA reveals the ability to obtain the highest transimpedance gain at the same consumed power. This result is predicted by both equation (38b) and (44b) and is stated in section II-G. In addition, the CR-RGC-TIA can achieve higher transimpedance gain compared to CR-TIA thanks to the regulation effect and the enhancement of the M_{n2} transconductance, see equation (46). However, this comes at the cost of decreasing the dynamic range because of the added regulating amplifier's noise.

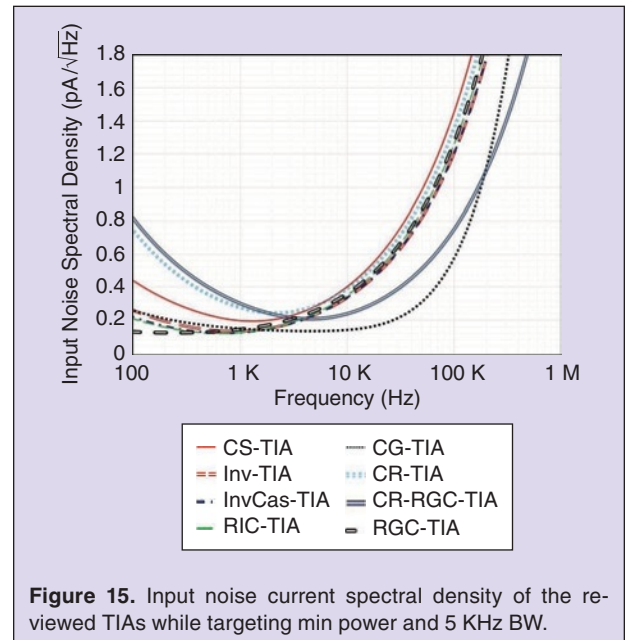
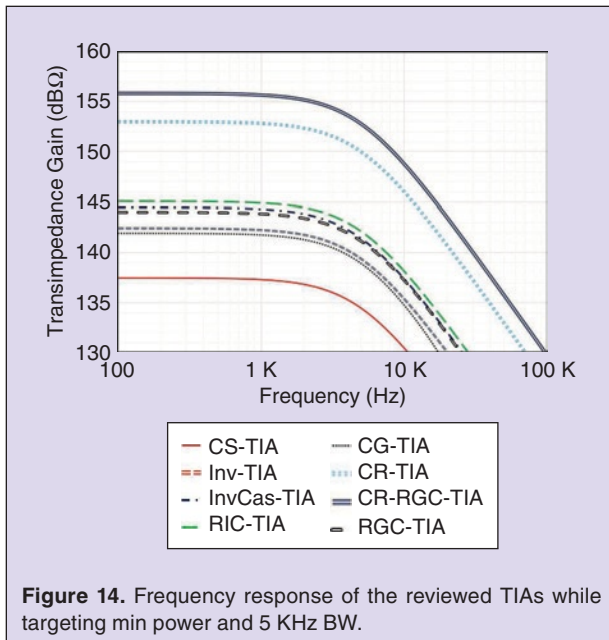
The simulation results of the CG-TIA and the RGC-TIA reveal that to operate in 5 KHz BW, those topologies have

to be biased with a very small current forcing the input transistor to operate in the weak inversion region. Thus, open loop topologies like RGC-TIA and CG-TIA are not a preferable option in low BW biomedical applications. Moreover, because the input referred noise current of the biasing current source is directly referred to the input, such topologies have the worst noise performance, see equations (31) and (37). Since the power consumption of the cascode transistor is very low (subthreshold operation), judging the performance by only FoM_1 can be deceiving. In addition, the power consumption of the RGC-TIA is two orders of magnitude higher than the CG-TIA because of the added regulating amplifier. Normally, the RGC-TIA would outperform in terms of GBW and FoM_1 if both topologies are operating in strong inversion, see sections III-C and III-D for the 100 MHz BW simulation results.

Furthermore, equations (31) and (37) show that there is no trade-off between power consumption and the input referred noise of both topologies. Therefore, the same results are stated in both of the presented minimum noise and minimum power cases for CG-TIA and RGC-TIA. Beside all that, the DR of the CG-TIA and the RGC-TIA is the worst among all of the compared topologies.

B. Case 2: $C_{PD} = 10$ pF, 5 KHz BW, Minimum Power

The frequency response and the input referred noise current spectral density of the reviewed TIAs are shown in Figs. 14 and 15 respectively. Also, a summary of the obtained simulation results for this case is listed in table X. Following the same comparison method used previously, RIC-TIA and InvCas-TIA achieve the highest GBW and the lowest power consumption at the same



input noise of Inv-TIA and CS-TIA. This is achieved because of the relatively high open loop gain and high effective transconductance of the core amplifier. Therefore, RIC-TIA and InvCas-TIA achieves the highest FoM₁ among the four topologies. The claim that higher open loop gain topologies obtain higher performance is also observed in this case as in the previous case; the Inv-TIA shows superiority over the CS-TIA.

However, since the aim of this simulation case is to minimize the power consumption, the DR, in general, is decreased compared to the previous case. Regarding the CR-TIA and the CR-RGC-TIA, both achieve the highest GBW of all studied topologies as in case 1. Also, the CR-RGC-TIA can achieve higher GBW at the expense of the input referred noise current and power consumption overhead compared to the CR-TIA.

C. Case 3: $C_{PD} = 2$ pF, 100 MHz BW, Minimum Noise

The frequency response and the input referred noise current spectral density of the reviewed TIAs are shown in Figs. 16 and 17 respectively. Also, a summary of the obtained simulation results for this case is listed in table XI.

A general rule of thumb regarding the four first topologies listed in the comparison table is that the higher the open loop gain the better the performance; similar to what is obtained in the 5 KHz BW results. The RIC-TIA and the InvCas-TIA exhibit the highest transimpedance gain and the highest FoM₁ as well among all of the eight topologies. This is achieved due to their large open loop gain and high effective transconductance of the core amplifiers' transistors. However, the RIC-TIA slightly outperforms the InvCas-TIA in term of

Topology	Gain (dBΩ)	BW (kHz)	Total Integrated Input Noise pA_{rms}	Power μW	I_{p-p}^{OVI} nA	DR (dB)	FoM1	FoM2
CS-TIA	138.1	5	13.6	85.2	80	75.4	346.7	27738.4
Inv-TIA	142.3	5	13.6	28.25	67	73.9	1695.9	113628.5
InvCas-TIA	144.3	5	13.6	14.9	42	69.8	4048	170017.7
RIC-TIA	145.1	5	13.6	19.8	41	69.6	3340	136946
CR-TIA	153	5	23.2	25	2.5	40.6	3850.7	9626.8
CR-RGC-TIA	155.8	5	23.2	68.7	1.3	35	1934.3	2514.6
CG-TIA	141.5	5	10.56	0.044	0.67	36	1279×10^3	857×10^3
RGC-TIA	144	5	14.3	6.8	0.53	31.4	8149.4	4319.2

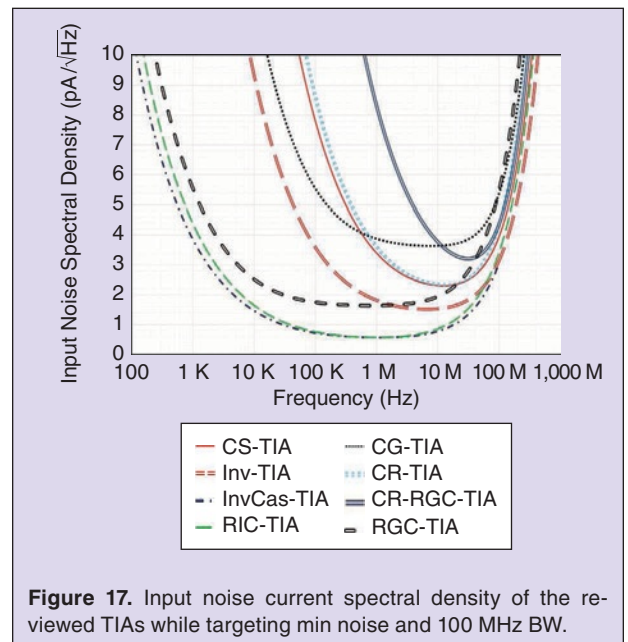
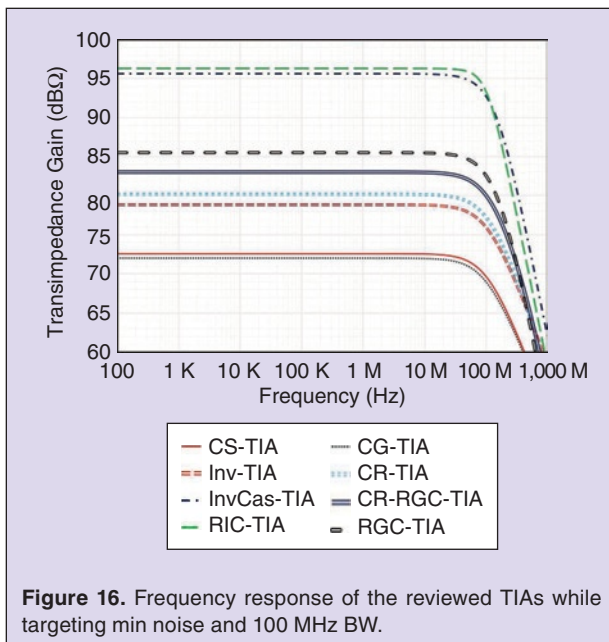


Table XI.

A comparison between the reviewed TIA topologies at $C_{PD} = 2$ pF and 100 MHz BW while targeting minimum noise.

Topology	Gain (dB Ω)	BW (MHz)	Total Integrated Input Noise nA _{rms}	Power μ W	I_{p-p}^{Ovl} μ A _{p-p}	DR (dB)	FoM1	FoM2
CS-TIA	72.6	100	33	570	99.1	69.5	45.3	4492.8
Inv-TIA	78.9	100	25.3	570	78	69.8	122.2	9531
InvCas-TIA	95.6	100	22.6	570	4	45	935.5	3742
RIC-TIA	96.3	100	24.6	570	1.1	33	931.6	1024.7
CR-TIA	80.2	100	35.5	570	0.93	28.4	101.1	94.1
CR-RGC-TIA	83.1	100	43	570	0.32	17.4	116.6	37.3
CG-TIA	72	100	45.8	100	55	61.6	173.8	9561.5
RGC-TIA	85.5	100	41.6	100	21	54.1	905.6	19017.6

GBW because of the former superior effective transconductance. On the other hand, the InvCas-TIA achieves higher dynamic range and slightly lower input referred noise at the same power consumption. Furthermore, the Inv-TIA has a better GBW and noise performance compared to the CS-TIA at the same consumed power. Both the CS-TIA and the Inv-TIA attain the highest DR due to their high I_{p-p}^{Ovl} .

Comparing the CR-TIA with the CR-RGC-TIA, the latter achieves higher transimpedance gain at the same power consumption. However, this comes at the expense of a higher input noise and lower DR. This explains why the design reported in [34] needed an automatic gain control to obtain a reasonable dynamic range for its intended biomedical application. In addition, CR-TIA and CR-RGC-TIA outperforms CS-TIA in terms of GBW and FoM₁ at the same consumed power. Also, CS-TIA has the superiority in term of FoM₂, linearity, and DR at the same power consumption.

At higher BW and relatively higher biasing current, the results of both CG-TIA and RGC-TIA become reasonable. Regarding the RGC-TIA, the regulation of the cascode transistor greatly boosts the effective transconductance resulting in a noticeably higher GBW compared to the CG-TIA. Consequently, the RGC-TIA outperforms the CG-TIA in all aspects except for the DR because of its higher transimpedance gain. One important observation is that the RGC-TIA achieves better noise performance at the same power consumption of the CG-TIA despite the extra components of the regulating amplifier. This is because the RGC-TIA needs less biasing current to attain the same effective transconductance for the cascode transistor; since g_{mn} is multiplied by $(|A_{rg}| + 1)$ as described by equation (33). Consequently, lower biasing current (lower g_{mnB}) means lower noise contribution from the dominant noise source (the biasing current source) which is directly proportional to g_{mnB} , see equation (37). Furthermore,

it is clear that the noise performances of the CG-TIA and the RGC-TIA are the worst among the studied topologies. Thus, it is advisable to avoid using CG-TIA and RGC-TIA if the input referred noise and the sensitivity are of the highest concern.

D. Case 4: $C_{PD} = 2$ pF, 100 MHz BW, Minimum Power

The frequency response and the input referred noise current spectral density of the reviewed TIAs are shown in Figs. 18 and 19 respectively. Also, a summary of the obtained simulation results for the minimum power case and 100 MHz BW is listed in table XII. Once again, higher open loop gain topologies achieves better performance regarding the first four topologies. InvCas-TIA achieves lower power consumption and higher GBW at the same input

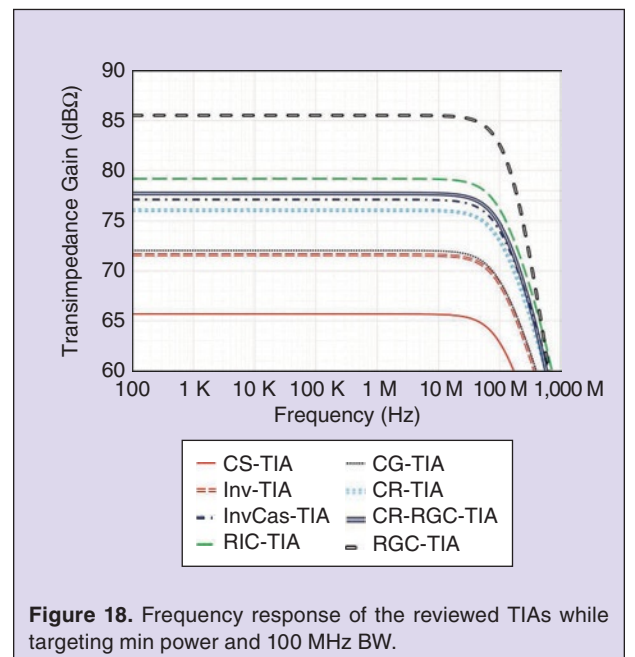


Figure 18. Frequency response of the reviewed TIAs while targeting min power and 100 MHz BW.

referred noise. However, higher transimpedance gain inherently limits I_{p-p}^{Ovl} which degrades the linearity and the dynamic range of the relatively higher open loop gain TIAs.

The CR-TIA and CR-RGC-TIA topologies achieves a higher GBW and FoM₁ compared to the CS-TIA. On the other hand, CS-TIA attains lower power consumption and better DR at the same achievable input referred noise current.

It is clear that the CG-TIA and the RGC-TIA are a very appealing choice when low power consumption is the main designer's concern. Clearly shown by the results, RGC-TIA noticeably outperforms all other topologies when minimizing the power consumption is the major goal. This superiority is obtained due to the high achievable effective transconductance of the cascode transistor at a relatively low DC biasing current. Thus, it is rec-

ommended to use the RGC-TIA if the noise performance requirements are not very constrained and the design has to be efficient in term of the power consumption, e.g., implantable devices.

IV. Conclusions

In this work, various state of the art TIAs mentioned in the literatures are outlined, analyzed, simulated, and compared. A noise and transimpedance gain mathematical models of all of the reviewed topologies are listed and discussed. For the first time, these studied topologies are simulated altogether at four different cases to account for a variety of design requirements and to allow a reasonable comparison methodology. The study outlined that for closed loop topologies, the higher the open loop gain, the higher the performance according to the figure of merit, FoM₁ described in this paper. This study also suggests that using transconductance boosting techniques like inverter based cascode and regulating cascode stages can greatly boosts the GBW performance of the TIA and reduces its input referred noise.

The InvCas-TIA and the RIC-TIA generally show great performance in terms of GBW, low input referred noise current, and low power consumption. Those two topologies are strongly recommended if the application sensitivity is of the major concern and they are optimized for minimum input referred noise. Moreover, both can achieve a relatively low power consumption while having a high open loop gain, thus, they can attain high transimpedance gain. Those aspects make both topologies very attractive for most of the biomedical applications. However, both topologies are not the best in terms of the DR especially at low power consumption.

On the other hand, CR-TIA and CR-RGC-TIA shows superiority over the CS-TIA in terms of GBW and FoM₁ at the expense of linearity, noise, and hence, the DR. In addition, the comparison shows that the noise performance

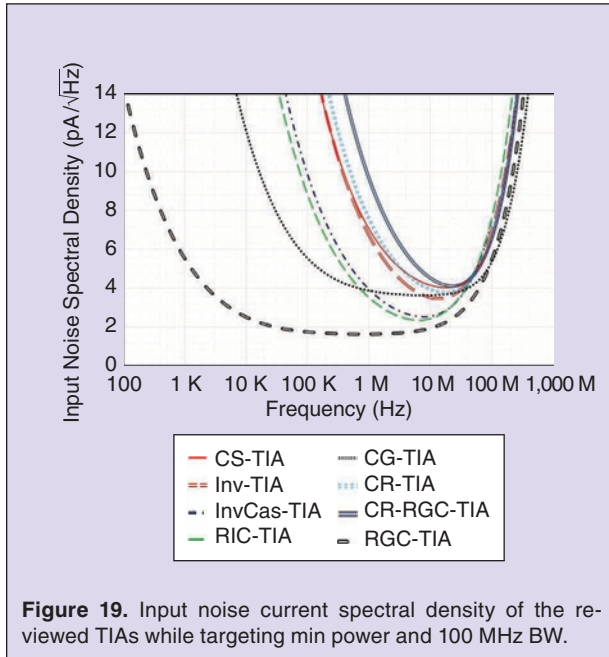


Figure 19. Input noise current spectral density of the reviewed TIAs while targeting min power and 100 MHz BW.

Table XII.

A comparison between the reviewed TIA topologies at $C_{pD} = 2$ pF and 100 MHz BW while targeting minimum power.

Topology	Gain (dBΩ)	BW (MHz)	Total Integrated Input Noise nA_{rms}	Power μW	$I_{p-p}^{Ovl} \mu A_{p-p}$	DR (dB)	FoM ₁	FoM ₂
CS-TIA	65.7	100	57	104.3	18	50	64.8	1167.2
Inv-TIA	71.6	100	57	143.7	78	62.7	92.8	7241
InvCas-TIA	77.1	100	57	101.3	9.4	44.3	248.1	2331.7
RIC-TIA	79.2	100	57	109	2.3	32.1	293.6	675.2
CR-TIA	76	100	57	188	1.1	25.7	117.8	129.5
CR-RGC-TIA	77.7	100	57	162	0.38	16.5	166.2	63.2
CG-TIA	72	100	45.8	100	55	61.6	173.8	9561.5
RGC-TIA	85.5	100	41.6	100	21	54.1	905.6	19017.6

Table XIII.
Summary and Recommendations.

BW	Target	In Term of FoM ₁	In Term of FoM ₂
5 KHz	Minimum Noise	CR-TIA CR-RGC-TIA	RIC-TIA InvCas-TIA
	Minimum Power	InvCas-TIA CR-TIA	InvCas-TIA RIC-TIA
100 MHz	Minimum Noise	InvCas-TIA RIC-TIA	RGC-TIA CG-TIA, Inv-TIA
	Minimum Power	RGC-TIA RIC-TIA, InvCas-TIA	RGC-TIA CG-TIA

of the current reuse topologies is the least at low BW. Thus, if the CR-TIA or the CR-RGC-TIA is the designer's choice, it is suggested to optimize for minimum noise performance to get a reasonable dynamic range.

The CG-TIA and RGC-TIA are the least preferred options for the low BW applications because they become more difficult to realize and require nA biasing current as R_D increases. Therefore, transistors have to operate in sub-threshold region which requires certain considerations, more accurate CAD models, and further fabrication trials to produce more reliable results.

In contrast, the study suggests that the CG-TIA and the RGC-TIA show great performance at higher BW especially when the main target is to minimize the power consumption. RGC-TIA can achieve high effective transconductance hence, high GBW at low power consumption.

In the context of the previous results, recommendations on what topology to use according to the required aspects are summarized in table XIII. The CG-TIA and RGC-TIA are not considered in the 5 KHz section of the following recommendation table because their extremely low power consumption would outshine their counterparts.



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An Alternative Path to Foster's Reactance Theorem and Its Relation to Narrow-Band Equivalent Circuits

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Abstract

Foster's seminal treatise on lossless networks has been published almost 100 years ago and a particularly notable conclusion drawn therein, i.e. that the reactance (and susceptance) functions are always monotonically increasing with frequency, is frequently referred to as Foster's theorem. In this paper we present two variants for an alternative simple derivation of a stronger form of this theorem, which holds for the driving point reactance (susceptance) of general lossless devices, i.e. also configurations without lumped elements. One version introduces a realizable lumped element equivalent circuit approximating the considered circuit in a narrow band around a particularly considered frequency. It turns out that this avenue of proof also facilitates an alternative validation of the realizability of the so called Foster 1 and 2 realizations.

I. Introduction

In 1924 Foster stated conditions for realizable immittances (i.e. impedances Z or admittances Y) of lossless networks (one-ports) composed of (potentially coupled) inductances L and capacitances C [1]. The impedance $Z=1/Y$ of such a network is purely imaginary $Z(\omega)=$

$jX(\omega)=1/(jB(\omega))$, where X and B denote the real-valued reactance and susceptance, respectively, which are functions of the (radian) frequency ω . Foster showed that the immittances are rational functions in $s=j\omega$ and that the associated partial fraction decomposition can be translated into realizable equivalent circuits, where terms corresponding to poles at particular frequencies $\pm\omega_x$ can be represented by a resonant LC (parallel or series) circuits. Poles at infinity or zero are represented by single inductances L or capacitances C and all these individual branches are connected in series or parallel when considering the partial fraction decompositions for Z and Y , respectively, as shown in Fig. 1. These canonical realizations are termed "Foster 1" and "Foster 2" circuits, respectively, and they represent equivalent circuits for the considered lossless network, which are valid in the entire frequency range. Example 1 (in a separate box) illustrates this procedure for a particular example.

While establishing a partial fraction decomposition for a rational function is a trivial step, the fact that the so derived circuit is actually realizable, i.e. that the resulting values for L and C are positive and real, is not self-evident and was proven by Foster. In literature, the term "Foster's theorem" is frequently associated with a

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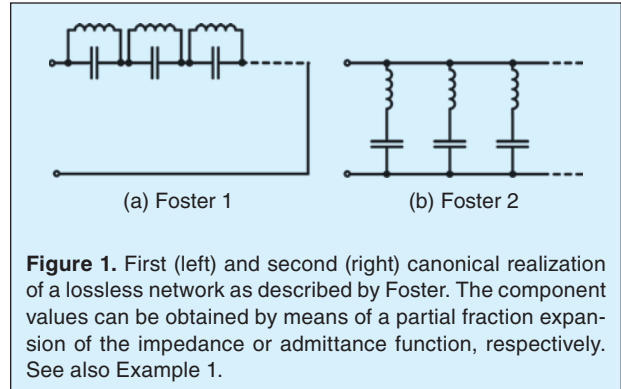
particular observation that was made in [1], i.e. that the reactance and susceptance functions always increase with frequency, which implies the poles and zeros of these immittance functions all lie on the real ω axis and alternate. This is frequently stated as¹

$$\frac{\partial X}{\partial \omega} > 0 \quad \text{and} \quad \frac{\partial B}{\partial \omega} > 0. \quad (1)$$

As pointed out by Foster himself [1], this property was actually proven earlier by Zobel [2] based on previous work of Campbell [3]. In fact, it can be shown that

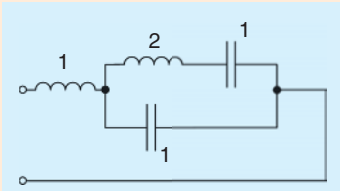
¹We provide the condition in the way it is usually cited. Strictly the “>” sign should rather be a “≥” sign as the degenerate case of a short or open circuit in principle also represents a lossless network.

Foster’s realization implies an even stricter requirement (see, e.g., [4], [5]), i.e.



Example 1

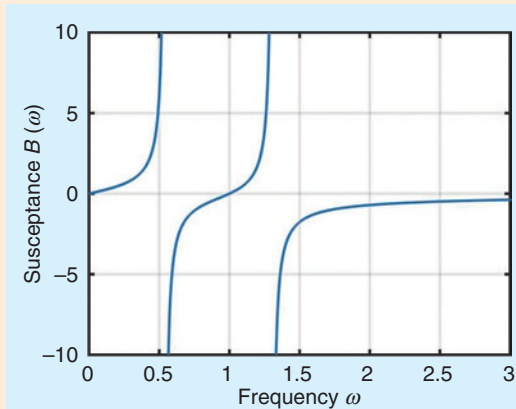
Consider the following lossless LC network (in all examples we consider suitably scaled, dimensionless quantities [9]):



The impedance of this network is given by

$$Z(s) = \frac{2s^4 + 4s^2 + 1}{2s^3 + 2s}$$

as can be readily verified. The susceptance versus frequency characteristics is given here



The partial fraction decompositions of this rational function yield for the impedance

$$Z(s) = s + \frac{1}{2s} + \frac{s}{2(s^2 + 1)}$$

and the admittance

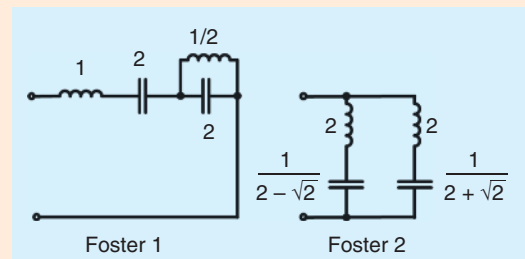
$$Y(s) = \frac{1}{2} \frac{s}{s^2 - s_1^2} + \frac{1}{2} \frac{s}{s^2 - s_2^2},$$

where

$$s_1^2 = -1 + \frac{1}{\sqrt{2}} \quad \text{and} \quad s_2^2 = -1 - \frac{1}{\sqrt{2}}$$

represent the two complex conjugate pairs of poles of $Y(s)$ (corresponding, in turn, to resonance frequencies). The poles of the impedance (at $\omega = 0$, $\omega \rightarrow \infty$ and $\omega = \pm 1$) appear as zeros of the admittance and vice versa.

Each term of these partial fraction decompositions can be represented by a resonant circuit in Foster’s equivalent circuit. In case of the decomposition for $Z(s)$ for this example (i.e., the “Foster 1” realization), the first two terms correspond to poles at infinity and zero yielding a single component rather than an LC tank.



The slope of the frequency response (of reactance or susceptance) is always larger or equal than that of an inductor or capacitor yielding the same reactance or susceptance at the particularly considered frequency.

$$\frac{\partial X}{\partial \omega} \geq \left| \frac{X}{\omega} \right| \quad \text{and} \quad \frac{\partial B}{\partial \omega} \geq \left| \frac{B}{\omega} \right|. \quad (2)$$

These conditions can be readily verified for the simple special cases of a single inductor (here the slope $\partial X/\partial \omega$ is simply given by the inductance L) and a single capacitance C , where $X = -1/(\omega C)$ and thus $\partial X/\partial \omega = 1/(\omega^2 C)$. We note that when passing frequencies where the susceptance or reactance functions show poles, the sign of these functions change from positive to negative but mathematically the derivative is non-existent at those “singular” frequencies such that the above conditions are not violated, i.e. they hold at all frequencies where the derivative exists.

In the years after its introduction, Foster’s theorem has been generalized to the case of electromagnetic fields (see, e.g. [6]) and considered in the context of many particular cases such as, e.g., resonant circuits [7] and the impedance of resonant antennas [8].

Foster’s proof given in [1] is based “upon the solution of the analogous dynamical problem of the small oscillations of a system about a position of equilibrium with no frictional forces acting”; thorough discussions of this approach can be found, e.g., in [4] and [9]. In [10] Papoulis provides an alternative proof based on the determinants associated with lossless networks of lumped elements. In [11] Nedlin² showed that the Foster condition (1) can alternatively be obtained by considering the average energy stored in a lossless network, when it is sinusoidally driven at a particular frequency.

In the following we will first show an approach similar to that in [11] for deriving the strict Foster condition (2) by considering the time-dependent energy taken up by a lossless network. Then we will discuss an approximate equivalent circuit valid in a narrow band around a chosen, particular frequency and use this equivalent circuit to again prove (2) in an even simpler manner. We also show that this equivalent circuit is always realizable (i.e. contains real-valued and positive component values). By considering Foster’s full equivalent circuit close to resonances, we finally show that from the previous considerations, it can also be proven that Foster’s equivalent circuit is always realizable, which yields an alternative path to Foster’s statements in [1].

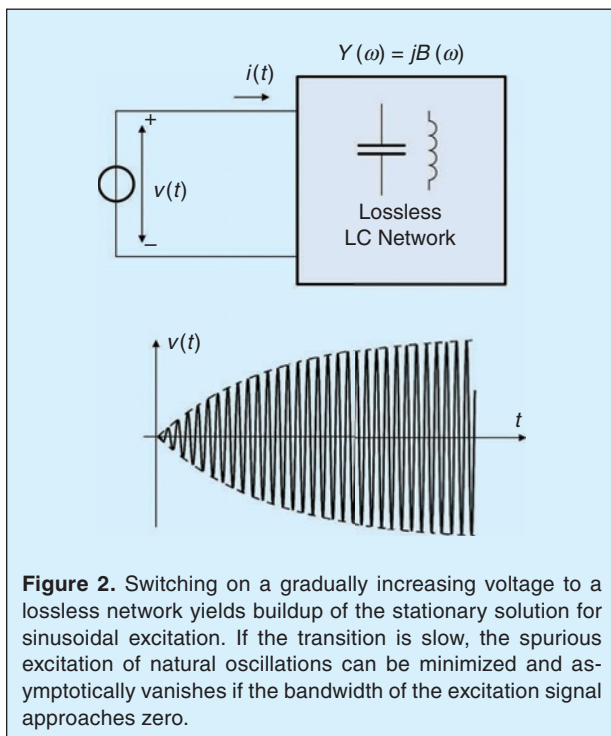
While the theorem has been proven before, the author feels that the presented approach is somewhat simpler to grasp and in particular does not require advanced complex analysis. Furthermore, the presented approach does not assume the network as being composed of lumped components which means that it also holds for systems featuring distributed components such as microwave resonators or transmission lines. Also, it illustrates the implications of the spurious excitation of natural modes of oscillations, which, in contrast to lossy networks, are undamped and thus infinitely sustained in purely reactive networks. As it turns out, only by carefully avoiding the excitation of these spurious oscillations, the reactance theorem can be obtained from this approach. And finally, an even simpler version of the proof can be obtained by considering equivalent circuits, which reproduce the reactance and its slope (with respect to frequency) accurately around a particularly chosen frequency, which are moreover, as mentioned above, always realizable and thus could also be used to represent the network in case of other narrow-band considerations.

II. Derivation of Foster’s Condition from Energy Considerations

As mentioned earlier, the following approach is similar to that presented in [11] but extends the consideration. It is also related to an approach presented by Paschke in his lecture notes [13], which, however, has never been published before to the best of our knowledge [14]. Note that the following approach does not consider that the network is composed of lumped circuit elements; the only assumption which is made is that no losses whatsoever occur in the one-port device.

When applying a sinusoidal signal to a lossless circuit (one-port), energy is provided to the circuit and transients occur, which depend on the manner the sinusoid is applied to the circuit, e.g., abruptly with a particular initial phase or with gradually increasing amplitude as it will be considered below. Once the stationary state has developed, we are faced with the well-known phenomena of reactive power, i.e. that at certain instants in time the network takes up power from the source while in others it provides power back to the source. In this stationary state, the *average* power taken up by the network vanishes, though. The way the sinusoidal signal is applied to the network in general makes a difference in the amount

²See also the comments on the paper in [12].

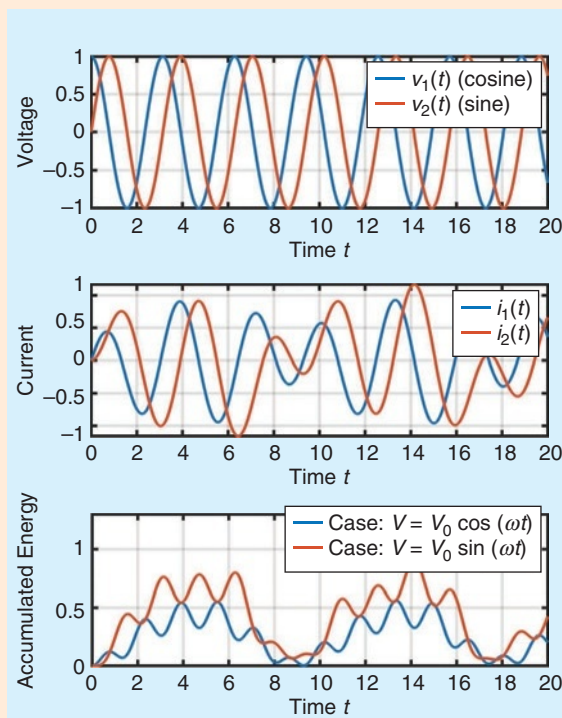


of energy that is transferred to the network during the transient phase. This can be easily demonstrated by considering the difference in transferred energy when abruptly switching on a cosine voltage or a sine voltage to an inductance at time $t = 0$. In the latter case (sine voltage), a DC offset current is superposed to the stationary current, which is associated to the well-known phenomenon of peak currents that may occur when transformers are connected to the line voltage. In lossy inductors, this offset current decays with time; in case of an ideal lossless inductor, however, it remains leading to a different amount of stored energy also in the stationary case (see also Example 2). These differences are associated with the natural oscillations of the network³ and can be avoided, if these are not excited at all, which is why this approach is considered in the following. Otherwise, also valid conditions could be derived, however, these would be network specific and would not yield the desired general Foster conditions introduced above.

To avoid such circumstances or ambiguities, we consider a sine (or cosine) signal, whose amplitude is only gradually increasing to a stationary value after switching on. In this case the corresponding spectrum occupies a very narrow band around the frequency of the underlying sinusoid. We define the applied voltage as

Example 2

The spurious excitation of natural oscillations can be illustrated by means of the network considered in Example 1. Abruptly applying a sinusoidal voltage $v(t)$ starting with $t = 0$ yields additional natural oscillations corresponding to the two poles of the susceptance⁴, where the strength of these oscillations depends on the initial phase of the sinusoid. This is demonstrated in the figures below for a cosine and a sine voltage. Integrating the instantaneous power $p(t) = v(t)i(t)$ over time yields the energy accumulated (stored) in the network at every instant of time. It can be clearly seen that (i) the characteristics depend on the excited natural oscillations and (ii) the energy is always larger or equal to zero, as expected.



$$v(t) = v_0(t) \cos \omega_0 t, \quad (3)$$

where the time-dependent amplitude (or envelope) $v_0(t)$ represents a slowly varying function in time featuring a very narrow spectrum $V_0(\omega)$ in frequency domain. The Fourier transform (FT) of $v(t)$ can then be written as

³In the aforementioned simple example of a single inductor, these natural "oscillations" occur at zero frequency, i.e. DC.

⁴When exciting the network by an ideal current source, the natural oscillations are determined by the zeros of the susceptance, i.e. the poles of the impedance.

$$V(\omega) = FT\{v(t)\} = \frac{1}{2}(V_0(\omega - \omega_0) + V_0(\omega + \omega_0)), \quad (4)$$

where, due to the multiplication in time domain, the spectral convolution of the FT of the cosine function (represented by delta functions located at $\pm\omega_0$) with $V_0(\omega)$ was considered. This spectrum represents a narrow-band signal around $\pm\omega_0$. When calculating the current that this voltage generates in a lossless admittance $Y(\omega) = jB(\omega)$, in view of the narrow band covered by the excitation voltage, we can approximate the susceptance function $B(\omega)$ around $\omega = \omega_0$ as

$$B(\omega) \approx B(\omega_0) + B'(\omega_0)(\omega - \omega_0), \quad (5)$$

Appendix A: Inverse Transform of the Current

The inverse Fourier transform of $I(\omega)$ can be obtained from the inverse Fourier transform of $V(\omega)Y(\omega) = jV(\omega)B(\omega)$, which, considering (4), reads

$$i(t) = \frac{j}{4\pi} \int_{-\infty}^{+\infty} \{V_0(\omega - \omega_0) + V_0(\omega + \omega_0)\} e^{j\omega t} B(\omega) d\omega. \quad (14)$$

Using the earlier discussed narrow-band approximation for the susceptance, we split the integral in two parts yielding

$$\begin{aligned} i(t) \approx & \frac{j}{4\pi} \int_{-\infty}^{+\infty} V_0(\omega - \omega_0) \{B(\omega_0) + B'(\omega_0)(\omega - \omega_0)\} e^{j\omega t} d\omega \\ & + \frac{j}{4\pi} \int_{-\infty}^{+\infty} V_0(\omega + \omega_0) \{B(-\omega_0) + B'(-\omega_0)(\omega + \omega_0)\} \\ & \times e^{j\omega t} d\omega. \end{aligned} \quad (15)$$

Using⁶ $B(-\omega) = -B(\omega)$ and $B'(-\omega) = B'(\omega)$, we can rewrite the second integral by substituting $\omega \rightarrow -\omega$. Considering further that⁶ $V_0(-\omega) = V_0^*(\omega)$, we can write the sum of both integrals in terms of the imaginary part of one integral yielding

$$\begin{aligned} i(t) \approx & \frac{j}{2\pi} \int_{-\infty}^{+\infty} V_0(\omega - \omega_0) \{B(\omega_0) + B'(\omega_0)(\omega - \omega_0)\} e^{j\omega t} d\omega \\ & \times \text{Im} \left\{ \int_{-\infty}^{+\infty} V_0(\omega - \omega_0) \{B(\omega_0) + B'(\omega_0)(\omega - \omega_0)\} e^{j\omega t} d\omega \right\}. \end{aligned} \quad (16)$$

Using the FT rules applying to frequency shifts and time derivatives, the inverse transform is then readily obtained as given in (6).

where $B'(\omega_0) = [\partial B / \partial \omega]_{\omega=\omega_0}$. A corresponding approximation can be applied around $\omega = -\omega_0$. Performing the inverse transform with these approximations then yields

$$i(t) \simeq -B(\omega_0)v_0(t)\sin(\omega_0 t) + B'(\omega_0)\dot{v}_0(t)\cos(\omega_0 t), \quad (6)$$

where $\dot{v}_0 = \partial v_0 / \partial t$. Details of the underlying straightforward calculation are given in Appendix A.

Next, considering that the instantaneous power delivered to the network can be obtained as $p(t) = v(t)i(t)$, we observe that integrating $p(t)$ from the moment the voltage starts building up, which we choose to be $t = 0$, to a particular time t_0 provides the energy that has been delivered to the network up to this time and this energy always has to be greater or equal than zero, i.e.

$$w(t_0) = \int_0^{t_0} i(t)v_0(t)\cos(\omega_0 t) dt \geq 0. \quad (7)$$

This requirement is based on the conservation of energy and, in particular, the passive character of our network, which, according to our assumptions, can only exchange energy with the outside world via the considered electrical port. Due to the assumed slowly varying envelope, the voltage is a narrow-band signal and we can use the approximation (6) to evaluate the integral. The integration can be performed in a straightforward manner by choosing a specific envelope function. A particularly simple result can be obtained by using the envelope

$$v_0(t) = \begin{cases} \hat{V}_0(1 - e^{-t/\tau}), & \text{for } t \geq 0, \\ 0, & \text{for } t < 0, \end{cases} \quad (8)$$

which, if $\omega_0\tau \gg 1$, corresponds to a very slow increase to the stationary state, which, in turn, is approached when $t_0 \gg \tau$.

Inserting (8) and (6) in (7), after some straightforward calculations outlined in Appendix B, yields the following asymptotic stationary result valid for $t_0 \gg \tau$

$$w(t_0) \simeq \frac{\hat{V}_0^2}{4} \left\{ \frac{B(\omega_0)}{\omega_0} \cos(2\omega_0 t_0) + B'(\omega_0) \right\} \geq 0. \quad (9)$$

This inequality must be fulfilled for arbitrary t_0 . As the cosine assumes values between -1 and $+1$ and the susceptance $B(\omega_0)$ may be positive or negative, in general, we readily obtain the condition (2) for the susceptance. Specifically, at times t_0 where the cosine equals $+1$, we obtain the condition $B'(\omega_0) \geq -B(\omega_0)/\omega_0$. For times, where the cosine equals -1 , we obtain $B'(\omega_0) \geq B(\omega_0)/\omega_0$. Depending on the sign of the susceptance, one of these conditions is more strict. As both must be fulfilled, we can combine them into a single inequality, i.e. (2). Similarly the condition for the reactance function can be

⁶The Fourier spectrum $X(\omega)$ of a real valued function $x(t)$ (such as a voltage, a current or impulse response) fulfills $X(-\omega) = -X^*(\omega)$, where the asterisk (*) denotes complex conjugation.

derived by applying a slowly increasing sinusoidal current rather than a voltage.

III. A Narrow-Band Equivalent Circuit and Another Derivation of Foster's Condition

Inspired by the previous approach, which considered the application of a narrow-band signal to build up a stationary state, we can ask what equivalent circuit would be suitable to represent a lossless network in a narrow band around some frequency ω_0 . It is well known that the admittance (or impedance) of a lossless circuit at a particular frequency ω_0 can be represented by a single equivalent inductance L_{eq} or capacitance C_{eq} by setting $B(\omega_0) = \omega_0 C_{eq}$ or $B(\omega_0) = -1/(\omega_0 L_{eq})$. However, when tuning the frequency ω away from ω_0 , the slope of the actual susceptance (reactance) will always be larger or equal than that of the equivalent component, which is a consequence of (2) and has also been noted by Bode in [5]. By composing the equivalent circuit out of two components, this shortcoming can be dealt with. In particular, it can be readily verified a parallel LC circuit with component values

$$C_p = \frac{1}{2\omega_0} (\omega_0 B'(\omega_0) + B(\omega_0)) \quad (10)$$

$$L_p = \frac{2}{\omega_0} \frac{1}{\omega_0 B'(\omega_0) - B(\omega_0)} \quad (11)$$

features the susceptance $B(\omega_0)$ and the slope $B'(\omega_0)$ at ω_0 and thus represents a narrow band approximation for the original lossless circuit. When a narrowband voltage is thus applied to this equivalent LC circuit, for decreasing bandwidth of the excitation signal, it will asymptotically take up the same power and thus also energy as the original circuit. If we assume a sinusoidal voltage that slowly builds up such as considered in the previous section (see Eqs. 3 and 8), we could thus again calculate the energy that is transferred to the circuit. However, we can spare the efforts of integration by simply summing up the well-known expressions for the energies stored in the components L_p and C_p in the stationary state, which, again, have to be greater or equal to zero at all times. In particular, for a stationary state voltage of $v(t) = \hat{V} \cos(\omega_0 t)$, using the well-known expressions for energies in L and C , we have

$$w(t) = \frac{C_p v(t)^2}{2} + \frac{L_p i_L(t)^2}{2} = \frac{\hat{V}^2}{2} \left(C_p \cos^2(\omega_0 t) + \frac{1}{\omega_0^2 L_p} \sin^2(\omega_0 t) \right) \geq 0, \quad (12)$$

where we considered that the current in L_{eq} is given by $i_L = \hat{V} \sin(\omega_0 t) / (\omega_0 L_p)$. Inserting the above values for the equivalent components, Eqs. 10 and 11, we obtain

$$w(t) = \frac{\hat{V}^2}{4} \left(B'(\omega_0) + \frac{B(\omega_0)}{\omega_0} \cos(2\omega_0 t) \right) \geq 0, \quad (13)$$

Appendix B: Evaluation of Integrals

The key lies in the asymptotic evaluation of the integrals under the conditions $\omega_0 \tau \gg 1$, which means that the envelope is very slowly increasing compared to the period $2\pi/\omega_0$ of the sinusoidal function, and $t_0 \gg \tau$, which accounts for the fact that we consider that the signals virtually assume the stationary state. Under these conditions the following asymptotic relations (and one identity), which will be used below, can be readily verified (α stands for n/τ with $n = 1, 2$ thus, in view of the assumptions above, we have $\omega_0 \gg \alpha$):

$$\begin{aligned} \int_0^{t_0} e^{-\alpha t} \sin(2\omega_0 t) dt &\simeq \frac{1}{2\omega_0}, \\ \int_0^{t_0} e^{-\alpha t} \cos(2\omega_0 t) dt &\simeq \frac{\alpha}{4\omega_0^2} \simeq 0, \\ \int_0^{t_0} e^{-\alpha t} dt &\simeq \frac{1}{\alpha}, \\ \int_0^{t_0} \sin(2\omega_0 t) dt &= \frac{1}{2\omega_0} (1 - \cos(2\omega_0 t_0)). \end{aligned} \quad (17)$$

Inserting (6) and the envelope (8) in (7), we obtain for the energy accumulated till time t_0

$$w(t_0) \simeq \hat{V}_0^2 \int_0^{t_0} \left\{ -B(\omega_0) (1 - e^{-\frac{t}{\tau}})^2 \sin(\omega_0 t) \cos(\omega_0 t) + B'(\omega_0) \frac{1}{\tau} e^{-\frac{t}{\tau}} (1 - e^{-\frac{t}{\tau}}) \cos^2(\omega_0 t) \right\} dt. \quad (18)$$

Expanding the brackets and using the trigonometric identities $\sin(2\beta) = 2 \sin(\beta) \cos(\beta)$ and $\cos^2(\beta) = (\cos(2\beta) + 1)/2$, by utilizing (17), we obtain the asymptotic solution given in (9).

where we used the identities $\cos^2 \beta + \sin^2 \beta = 1$ and $\cos^2 \beta - \sin^2 \beta = \cos(2\beta)$. The obtained inequality is the same as the one obtained in (9) before and thus also directly leads to Foster's condition (2).

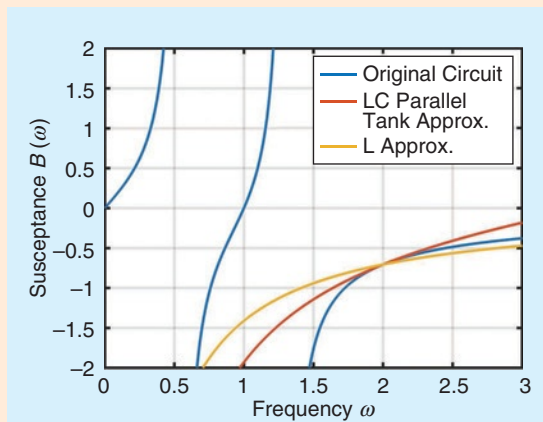
Thus far, we have not considered the question, whether the component values of the equivalent circuit are positive and if the equivalent circuit thus would be realizable⁵. Inserting the obtained conditions in (10) and (11), it turns out that the component values L_p and

⁵Note that this does not affect the energy consideration as a fictitious negative inductor or capacitor would simply be a component that can provide energy to the external circuitry. This energy could be overcompensated by the other component such that the equivalent circuit in total could, in principle, still be passive.

C_p are always positive, which means that this narrow band equivalent circuit for a lossless network is always realizable! We finally note that in a similar manner a corresponding conclusion can be made for an equivalent circuit featuring an LC series circuit. Example 3 shows the characteristics of the different approximations for our worked example in a susceptance versus frequency plot.

Example 3

The graph below shows the quality of the narrowband approximation for the susceptance associated with the example network (see Example 1) by means of an LC parallel tank in comparison to the approximation by a single inductance. The approximation has been performed for $\omega_0 = 2$, where the susceptance values of the exact characteristics and the approximations coincide. However, the LC parallel tank also correctly reproduces the slope of the susceptance spectrum at $\omega_0 = 2$, which means that it represents the network truthfully for narrowband signals. Accordingly, when applying a narrowband signal leading to the stationary state, the energy stored in the network can be calculated from this approximately equivalent LC tank. Also, when approaching a parallel resonance frequency, in this example at $\omega = 1$, the values L_p and C_p obtained for the approximation at the considered frequency asymptotically match the LC parallel tank corresponding to this resonance frequency in the "Foster 1" realization. As it was proven that L_p and C_p are always greater or equal to zero (and thus represent a realizable network), it is therefore also proven that the components in the Foster 1 realization are always greater or equal to zero.



IV. Further Relations to Foster's Original Conditions

In the above sections we showed, how the consideration of the energy that is stored in the lossless network after building up the stationary state can lead to Foster's conditions (1) and (2). In fact, Foster's paper [1] provides much more than this condition. It provides the well-known equivalent circuits, i.e. Foster's first and second form of a canonical realization as shown in Fig. 1, which can be related to a partial fraction decomposition of the immittance functions as discussed above and illustrated in the examples.

Foster's equivalent circuits feature resonant LC circuits corresponding to natural modes of oscillations. As every lossless LC circuit can, in principle, indefinitely sustain oscillations, the total energy contained in the network depends on the potential excitation of these natural modes and thus on the way the stationary state was approached. Which particular natural modes of oscillation are actually excited crucially depends on the driving circuit. For instance, including an internal resistance in the chosen source introduces losses in the entire circuit, i.e. the LC network and source network, and thus potentially excited natural oscillations can be dampened such that they vanish as time progresses. Alternatively, the excitation of these natural modes can be avoided if the spectrum of the excitation signal features no significant contributions at the frequencies associated with these natural modes of oscillation, which is the consideration that led us to the application of a slowly increasing sinusoid above.

As mentioned in the Introduction, while the partial fraction expansion of a rational function, i.e. the immittance function, and the interpretation of individual terms as resonant LC circuits in an equivalent circuit is straightforward, it is not obvious that the resulting LC component values are real-valued and positive and that the equivalent circuit thus corresponds to an actually realizable one - this fact was explicitly proven by Foster.

This proof can also be provided by virtue of narrow band approximation introduced in the previous section. The considered approximate parallel LC circuit also features a resonance, which, in general, is of no physical significance, though. The circuit merely approximates the admittance (and thus also impedance) of the original circuit in a narrow band around the particularly selected driving frequency ω_0 . However, if ω_0 is chosen to approach one of the parallel resonance frequencies of the circuit (where the susceptance $B(\omega)$ approaches zero), the equivalent approximate circuit will asymptotically represent one of the

LC tanks shown in the “Foster 2” realization Fig. 1 (left). As we have proven that the component values for this equivalent circuit are always real and positive, this also means that the component values of the “Foster 1” circuit have to be positive. A similar consideration can be made using an approximate LC series (rather than parallel) circuit yielding the realizability of the components for the “Foster 2” circuit when considering frequencies featuring series resonance (i.e. vanishing reactance $X(\omega)$). Hence, besides the reproduction of the conditions (2), this approach also provides a simple alternative proof for the realizability of Foster’s equivalent circuits.

V Conclusion

It was shown that the property that the reactance and susceptance of a lossless network always increases with frequency, which is frequently referred to as Foster’s theorem, can be derived by considering the amount of energy that is delivered to the network when building up the stationary state. This method readily proves the more stringent version of the theorem stating that the slope of the frequency response (of reactance or susceptance) is always larger or equal than that of an inductor or capacitor yielding the same reactance or susceptance at the particularly considered frequency. Also, this consideration is not restricted to lossless networks composed of lumped elements.

This particular approach has also led to the consideration of an equivalent LC circuit that yields a narrow band approximation of the frequency responses by not only yielding the correct value of the reactance or susceptance, but also the correct slope. Foster’s condition can be readily deduced by considering the energy in these equivalent components. It was also proven that these equivalent components are always positive and thus the narrow-band equivalent circuit is always realizable. As the equivalent LC circuit (series or parallel) converges to one of the resonant LC circuits in Foster’s equivalent circuits when approaching a particular resonance frequency, this can also be used to prove the realizability of Foster’s circuits (type 1 and type 2).

In summary, the presented framework provides a simple alternative route to Foster’s theorem.

Acknowledgment

The author is deeply indebted to Fritz Paschke, a dedicated scientist, inventor and teacher, who inspired the considerations in this paper a long time ago and who presented a special version of this approach in his lectures at Vienna University of Technology [13].

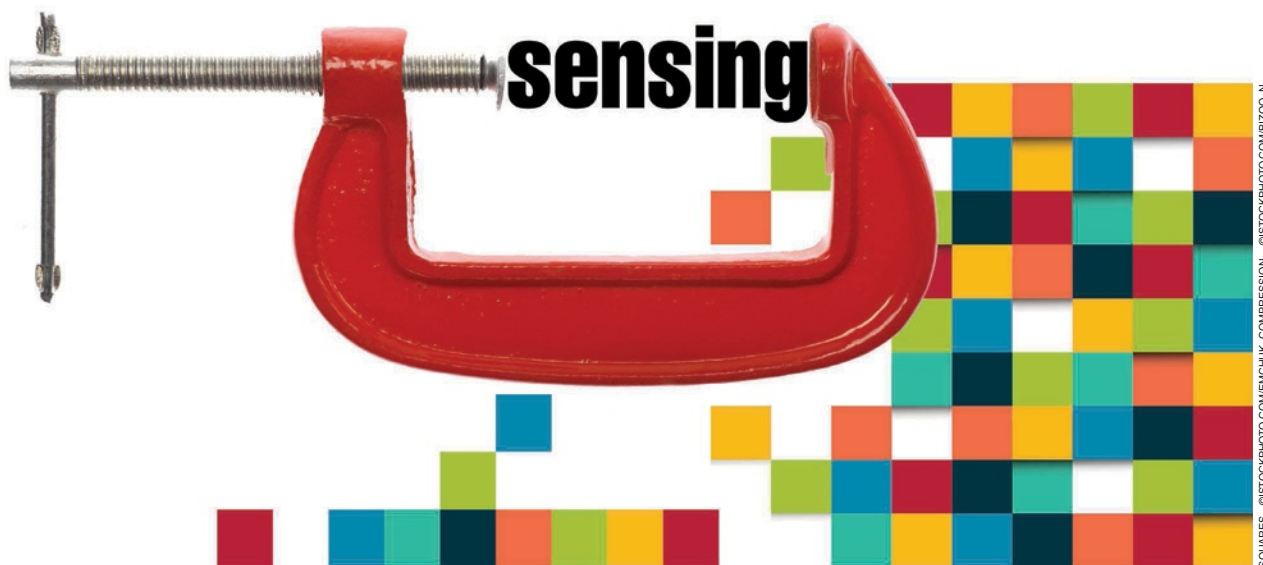


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Adapted Compressed Sensing: A Game Worth Playing



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Abstract

Despite the *universal* nature of the compressed sensing mechanism, additional information on the class of sparse signals to acquire allows adjustments that yield substantial improvements. In facts, proper exploitation of these priors allows to significantly increase compression for a given reconstruction quality.

Since one of the most promising scopes of application of compressed sensing is that of IoT devices subject to extremely low resource constraint, adaptation is especially interesting when it can cope with hardware-related constraint allowing low complexity implementations.

We here review and compare many algorithmic adaptation policies that focus either on the encoding part or on the recovery part of compressed sensing. We also review other more hardware-oriented adaptation techniques that are actually able

to make the difference when coming to real-world implementations. In all cases, adaptation proves to be a tool that should be mastered in practical applications to unleash the full potential of compressed sensing.

I. Introduction

All the *magic* of Compressed Sensing (CS) [1] is in the possibility of going back and forth between two vectors $\mathbf{x} \in \mathbb{R}^n$ and $\mathbf{y} \in \mathbb{R}^m$ with $m < n$ providing the first is κ -sparse ($\kappa < m$). This means that an $n \times d$ matrix \mathbf{D} called *dictionary* exists such that the instances of \mathbf{x} can be expressed as $\mathbf{x} = \mathbf{D}\boldsymbol{\xi}$ with $\boldsymbol{\xi}$ having not more than κ non-zero entries.

We go from \mathbf{x} to \mathbf{y} (the *encoding* step) with a linear transformation $\mathbf{y} = \mathbf{A}\mathbf{x}$ for a certain $m \times n$ matrix. We go from \mathbf{y} to \mathbf{x} (the *decoding* step) by exploiting the sparsity

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prior on \mathbf{x} to pick the right element among the infinite set of solutions in ξ of the linear systems of equalities $\mathbf{y} = \mathbf{A}\mathbf{D}\xi$. The key point in decoding is that the search for a sparse solution can be translated into a convex optimization problem that can be tackled either exactly or by means of some iterative approximation [2].

Compressed sensing is no longer an utterly new topic as the seminal papers of Donoho, Candes and Tao [2]–[4] that shed light upon this double path date back not less than 12 years.

The amount of theoretical development in this field is impressive as is the number of techniques used for reconstructing the so called *original signal* \mathbf{x} from the overly famous *small number of linear measurements* in the vector \mathbf{y} [5]–[9].

Among all the methodological results, *adaptation* has always been given a secondary role. The very main theory of CS centers on words such as *universal*, *democratic*, *non-adaptive*, etc. Actually, the pairing of sparsity with linear encoding is such a powerful concept that all the theoretical guarantees that ensure CS to work are basically independent of the specific features of the signals involved in the process.

This is a key observation. In fact, a direct consequence of this approach is that typical theoretical guarantees are upper bounds on reconstruction errors, and upper-bounding means that a worst-case analysis has been carried out, and worst-case analysis implicitly considers also the *worst* possible signals, whatever it may mean in each specific context.

From a more applicative point of view, guarantees are fundamental, but signals are not as bad as one is forced to assume in the worst-case analysis. On the contrary, most of the times they have features in addition to sparsity that can be leveraged through adaptation to increase system performance. This is especially important in case of hardware implementations that, by their nature, must maximize performance while complying with possibly severe resource constraints.

Hence, while universal theories deal with asymptotic trends, adaptation allows the tuning of the *constant coefficients* hidden in the asymptotic trend formulas that are irrelevant in the run to infinity, but largely affect the cost and the performance of real-world systems.

This playing with constants can be a key factor in expressing the practical potential of CS. In fact, the ultimate simplicity of the encoding step hints at applications in which resources at the acquisition side are scarce while computational power is available at the receiver of the sensed information. This perfectly fits within the general framework that most of the information engineering

community is working on, i.e., the grand view implied by “memes” like *Internet of Things* (IoT) or *Cyber-Physical Systems* (CPS).

Networks of ubiquitous sensors and actuators whose activity entails an intense exchange of data between them and to local hub infrastructures, that act as a gateway to cloud-based processing and decision, and in which acquired signals follow a path that goes from extremely simple sensing units, to concentrators, to server farms. The ability to compress with a limited resource budget is appealing both at individual nodes and in gateways, and CS can be a winning option.

This review article aims at collecting the most widespread adaptation techniques presented in literature which proved capable of improving CS performance on real-world signals and of making the implementation of the acquisition subsystems of IoT networks more effective. We concentrate on *adapted* CS and not on *adaptive* CS, meaning that *adaptation is performed at design-time* considering the class of signal to acquire and *not at run-time* on each signal instance [10]. Roughly speaking, adapted CS methods do not require any resource trade-off. Encoding procedures are still based on the matrix multiplication $\mathbf{A}\mathbf{x}$, with the advantage to (strongly) reduce the number of rows in \mathbf{A} . With respect to the adoption of the standard CS theory, the produced benefits are both higher data compression and lower computational burden of the encoder. Though we tried to be as exhaustive as possible in bibliographic search, not every contribution is reported here as we concentrate on those that appear to give better performance.

As a teaser on what can be done following this path, consider a case leveraging on the simplicity and flexibility of CS, whose performance can be substantially boosted by adaptation. Electro Cardio Graphics (ECG) signals are of interest in both healthcare and wellness oriented applications as they give information on the status of the hearth as well as on the activity of the subject.

The general effectiveness of CS in ECG monitoring is discussed, for example, in [11], that shows a $\approx 40\%$ improved battery lifetime compared to state-of-the-art compression techniques for an embedded ECG monitor although no adaptation is considered.

The approach discussed in [12] uses CS as a basic building block for ECG compression simultaneously supporting both health care and wellness applications in a dual-mode wearable monitor. More specifically, CS is employed as low-resource scalable lossy compression stage working immediately after signal digitalization and before data dispatching. From $\mathbf{y} = \mathbf{A}\mathbf{x}$ one gets that each measurement in the vector \mathbf{y} contains information

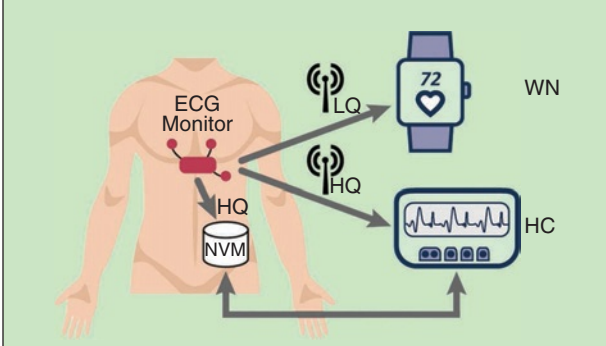


Figure 1. A dual mode ECG monitor that locally stores compressed data for medical-grade analysis while a subset of the compressed data are transmitted to a gateway for wellness oriented applications.

on the whole vector \mathbf{x} and thus the number of measurements passed to the decoder is a simple but effective way of administering the rate-distortion trade-off.

As reported in Figure 1, the monitoring device is equipped with a Non-Volatile-Memory (NVM) that stores the m^{HQ} measurements needed to reconstruct an High-Quality medical-grade ECG (HQ) and with a transmitter sending only $m^{\text{LQ}} < m^{\text{HQ}}$ of those measurements to a personal device, such as a smartwatch or a smartphone, whose functionalities depend on the reconstruction of a Low-Quality ECG (LQ), e.g., sufficient to reliably estimate heart rate. Actually, the proposed device can switch from LQ to HQ due to an external trigger either from the patient or from the heart rate monitoring device in case of critical events whose scrutiny is needed at medical-grade precision.

Clearly, both storage and transmission take advantage of compression in terms of hardware cost, memory footprint, computation time and, most important, energy consumption. Adaptation plays a fundamental role in this. In fact, once target qualities are fixed, the adoption of classical CS like in [11] compresses with a factor 2.2:1 in the HQ setting and 3.7:1 in the LQ setting. If methods among these presented in this paper are employed, the above figures become a compression ratio of 6.0:1 for the HQ setting and 14.2:1 in the LQ setting.

The illustrated application briefly highlights how the adaptation can be directly employable in the design of market-ready systems. This is also an example of the way in which we expect adaptive CS to play a significant role in the incoming future.

As an additional example, it is also worth mentioning that the U.S. Food and Drug Administration has recently approved a magnetic resonance imaging scan¹ that uses CS to speed up the images acquisition.

¹online available on: <https://www.healthimaging.com/topics/cardiovascular-imaging/fda-clears-compressed-sensing-mri-acceleration-technology-siemens>

The rest of the paper is organized as follows. Section II reports the basics of CS and three of the most useful explanation of its working principle. Section III is devoted to the review of methods that adapt the encoder to the class of signals to acquire, distinguishing between methods inspired by mutual coherence arguments and methods driven by average energy considerations. Improvements with respect to non-adaptive CS provided by encoder adaption are assessed in Section IV. Section V deals with adaptation at the decoder. Section VI develops the ECG monitoring application sketched above by applying the best performing methods both at the encoder and at the decoder. Section VIII is finally devoted to describe adaptation policies that were devised in CS hardware implementations.

II. Basics of CS

The most general model for CS signal encoding is $\mathbf{y} = \mathbf{A}(\mathbf{x} + \mathbf{v}^x) + \mathbf{v}^y$, where $\mathbf{v}^x \in \mathbb{R}^n$ and $\mathbf{v}^y \in \mathbb{R}^m$ are vectors of disturbances corresponding to the errors implicitly attached to the signal (\mathbf{v}^x) and those due to the processing producing the measurements (\mathbf{v}^y).

For simplicity's sake, most of the contributions that tune \mathbf{A} neglect \mathbf{v}^x as it makes the overall disturbance contribution $\mathbf{A}\mathbf{v}^x + \mathbf{v}^y$ dependent on \mathbf{A} . We adhere to such a simplification, neglect such a dependency, and assume $\mathbf{y} = \mathbf{A}\mathbf{x} + \mathbf{v}$ where \mathbf{v} is a vector of white and Gaussian disturbances $\mathbf{v} \sim \mathcal{N}(\mathbf{0}, \sigma^2 \mathbf{I}_m)$, with \mathbf{I}_m the $m \times m$ identity matrix and σ^2 the power of the equivalent noise affecting each measurement. Paired with that, the prototype decoding algorithm is the so called basis pursuit denoising (BPDN) that estimates $\hat{\mathbf{x}} = \mathbf{D}\hat{\xi}$ with

$$\hat{\xi} = \underset{\xi \in \mathbb{R}^d}{\text{argmin}} \|\xi\|_1 \quad \text{s.t.} \quad \|\mathbf{y} - \mathbf{B}\xi\|_2 \leq \eta \quad (1)$$

where $\|\cdot\|_p$ indicates the p -norm, $\mathbf{B} = \mathbf{A}\mathbf{D}$ and $\eta = \max\|\mathbf{v}\|_2$ takes into account the maximum deviation from the original signal due to disturbances. Assuming that $\mathbf{x} = \mathbf{D}\xi$ for a certain ξ one aims at $\hat{\xi} = \xi$.

To grasp the core of CS theory, assume first that $\eta = 0$, the noiseless case in which BPDN reduces to Basis Pursuit (BP). Since $m < n$, then \mathbf{A} and \mathbf{B} are slanted matrices and, assuming that they are full rank, finding $\hat{\xi}$ means picking the right solution among the infinite number of candidates that satisfy the ill-conditioned system of equations $\mathbf{y} = \mathbf{B}\xi$.

A. Explaining CS With Restricted Isometries

First, let us try to explain how the previous problem may admit a solution by assuming that matrix \mathbf{B} satisfies the well-known Restricted Isometry Property (RIP) [13]. Start by noting that an obvious requirement is that no two κ -sparse vectors $\xi' \neq \xi''$ solve $\mathbf{y} = \mathbf{B}\xi_j$. In fact, if $\mathbf{y} = \mathbf{B}\xi' = \mathbf{B}\xi''$, i.e., if $\mathbf{B}(\xi' - \xi'') = 0$, it is impossible to tell from \mathbf{y} which of the two solutions is the true signal.

Going back to the noisy case $\eta > 0$, not to be fooled by disturbances, one should require that for any two κ -sparse vectors $\xi' \neq \xi''$, the two vectors $B\xi'$ and $B\xi''$ are sufficiently far apart, i.e., that $B(\xi' - \xi'')$ is not too small.

Since if ξ' and ξ'' are κ -sparse, then $\xi' - \xi''$ is up to 2κ -sparse, and we need B to behave in a *proper way* when applied to 2κ -sparse vectors.

This is formalized by the definition of the RIP that requires B to be almost an isometry (i.e., a transformation that preserves length) when it is applied to 2κ -sparse vectors. RIP is quantified by a Restricted Isometry Constant (RIC) $\delta_{2\kappa}$ that is 0 when B is a true isometry and increases as B departs from that condition.

These ideas have been able to originate the most widely known guarantees on the possibility of reconstructing x from y by means of (1) [3]. By largely simplifying the sophisticated machinery needed to prove this result, one knows that if $\delta_{2\kappa} \leq \sqrt{2} - 1$ the reconstruction error is bounded from above and thus cannot completely disrupt the signal. In the noiseless case $\eta = 0$ the reconstruction can be perfect, and the guarantees substantially depend on the same assumption on $\delta_{2\kappa}$.

Furthermore, one can also prove that, if $m = O(\kappa \log(n/\kappa))$ and one chooses A as a $m \times n$ random matrix whose entries $A_{j,k}$ are independent and identically distributed (i.i.d.), for example, as normals (i.e., $A_{j,k} \sim N(0,1)$), then the probability of producing a matrix B that satisfies the RIP property is extremely high independently of the choice of the dictionary D .

These good news imply a very simple design flow that is completely agnostic of the features of the signal to acquire with the exception of its sparsity κ , and basically employs i.i.d. random matrices with the proper size.

Yet, since such a design flow is based on guarantees and thus on worst-case derivations, *in practice the performance of this kind of CS systems on typical signals is much better than what is ensured by theory.*

B. Explaining CS With Mutual Coherence

Figure 2 helps understanding how CS works by applying it to the particular case $n = d = 3$, $m = 2$ and $\kappa = 1$.

As a general property, any B decomposes its n -dimensional domain into two orthogonal subspaces: its $(n - m)$ -dimensional kernel $\ker B$ (the green line on the left of Figure 2) and the m -dimensional image subspace $\text{im} B^\top$ (the green plane on both sides of Figure 2). Since vectors in $\ker B$ disappear in the mapping, multiplication by B amounts to projection onto $\text{im} B^\top$. Vice versa, once we are given a measurement vector y' , the equation $y' = B\xi$ defines the affine $(n - m)$ -dimensional subspace spanned by the sum $B^+y' + e$ (where B^+ indicates pseudo-inversion) for any $e \in \ker B$ and represented,

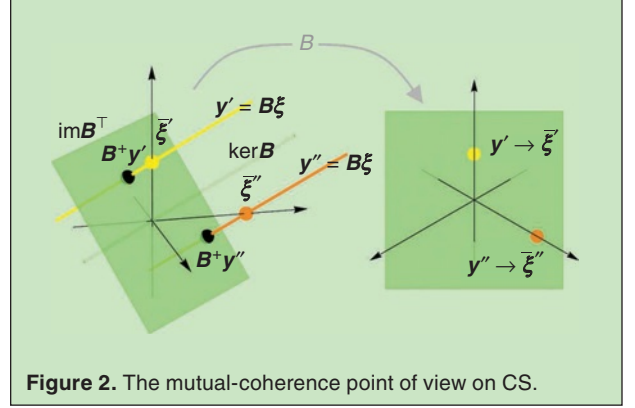


Figure 2. The mutual-coherence point of view on CS.

for example, by the yellow straight line in Figure 2. Since $\kappa = 1$, among all the points of such subspace, the one corresponding to the signal is that sitting on a coordinate axis, i.e. the ξ' represented by a yellow dot in Figure 2.

The same happens for the other measurement vector y'' , that defines the orange affine subspace $B^+y'' + e$ of Figure 2 which contains only one point sitting on a coordinate axis, i.e., the orange dot representing ξ'' .

Clearly, this going from y to ξ is possible since the projections of the coordinate axis on the green plane are distinct, as shown on the right of Figure 2 that represents the co-domain of B .

In more general terms, since $y = B\xi$, such projections are the columns of B . Since we are dealing with n vectors in an $m < n$ -dimensional space, they cannot be orthogonal. Yet, we may ask them to be “as orthogonal as possible”. This is where *mutual coherence* [14] comes into play. It is defined considering the columns vectors $B_{\cdot,0}, \dots, B_{\cdot,n-1}$ and setting

$$\mu(B) = \max_{j \neq k} \frac{|B_{\cdot,j}^\top B_{\cdot,k}|}{\|B_{\cdot,j}\|_2 \|B_{\cdot,k}\|_2} \quad (2)$$

Mutual coherence is the cosine of the smallest angle between any two vectors $B_{\cdot,j}$ and is bounded by $\mu_{\min} \leq \mu(B) \leq 1$ with $\mu_{\min} = \sqrt{(d-m)/(d-1)m}$ [15]. In our toy case, the perfectly symmetric disposition of the 3 projections in the 2-dimensional plane, implies $\mu(B) = 1/2^2$ that matches the lower bound for $d = n = 3$ and $m = 2$ thus making B a very good matrix for CS.

The most well-known result linking mutual coherence with the possibility of reconstructing x from y is that, in the noiseless case, BP recovers the correct original signal providing that $\mu(B) \leq 1/(2\kappa - 1)$ [16].

In general, to cope with possible disturbances that offset the measurement vectors from its ideal position, one

² that corresponds to angles of $2/3\pi$ between each pair of vectors in Figure 2

should choose the matrix \mathbf{A} so that the mutual coherence of the columns of $\mathbf{B} = \mathbf{A}\mathbf{D}$ is as low as possible to keep the projections of the axes as far as possible from each other.

C. Explaining CS With Polytopes

An interesting alternative view on noiseless recovery comes from a polytope interpretation of BP whose working principle can be exemplified using the same toy case used above. The 1-norm sphere of radius r , i.e., $\{\xi \in \mathbb{R}^n \mid \|\xi\|_1 \leq r\}$, is the so-called n -dimensional *cross-polytope*. For $n = 3$ is its the blue diamond-like shape in Figure 3.

In that figure, the radius of the 1-norm sphere is the minimum allowing a non-empty intersection between the sphere itself and the yellow line, an intersection that is the solution of BP. Note that this intersection contains the true ξ^* but only a properly designed \mathbf{B} can guarantee that other solutions do not exist.

In particular, since $\kappa = 1$, the solution is on a vertex of the cross-polytope that must be identified starting from the projection $\mathbf{B}^+\mathbf{y}$ on the green plane.

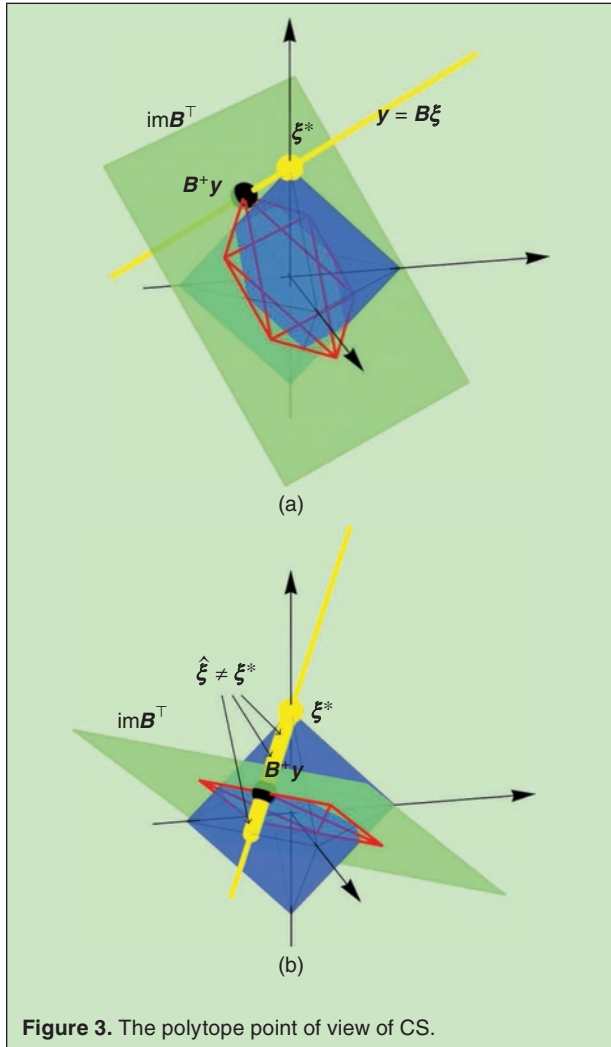


Figure 3. The polytope point of view of CS.

In the case of Figure 3(a) the projection of the cross-polytope on the green plane yields the red hexagon in which the 6 vertices of the cross-polytope are still distinguishable.

On the contrary, in Figure 3(b) the projection of cross-polytope on the green plane is the red rectangle in which 2 of the 6 vertices of the cross-polytope disappear.

When this happens, more than one point of the minimum-radius cross-polytope projects on the same $\mathbf{B}^+\mathbf{y}$ and BP is unable to ensure that its solution is sparse and thus coincides with the true signal.

This can be generalized to generic κ -sparse signals sitting on κ -dimensional facets of the cross-polytope, which in this case should be projected on the subspace $\text{im}\mathbf{B}^\top$ and remain distinguishable. This leads to the estimation of the probability that reconstruction is possible as the ratio between the number of facets that are still recognizable after projection over the total number of facets.

Overall, if one adopts this point of view, good matrices \mathbf{A} are those for which $\mathbf{B} = \mathbf{A}\mathbf{D}$ preserves distinguishability of κ -dimensional facets of the n -dimensional cross-polytope.

Adaptation methods start from the theoretical developments that we have just sketched and identify promising merit figures that are related with the capability of effectively reconstructing ξ^* from \mathbf{y} . Then, propose heuristics to improve such merit figures.

III. Adaptation at the Encoder Side

In describing all the methods we adopt some common notation. Given a possible sensing matrix \mathbf{A} , the matrix $\mathbf{B} = \mathbf{A}\mathbf{D}$ and the Gram matrix $\mathbf{G} = \mathbf{B}^\top\mathbf{B}$ remain implicitly defined. Given any matrix \mathbf{M} , we indicate its Singular Value Decomposition (SVD) as $\mathbf{M} = \mathbf{U}_M\mathbf{\Lambda}_M\mathbf{V}_M^\top$ with \mathbf{U}_M and \mathbf{V}_M orthonormal matrices and where $\mathbf{\Lambda}_M$ the diagonal matrix aligning the singular values $\lambda_{M0} \geq \lambda_{M1} \geq \dots \geq 0$. In what follows, when a matrix \mathbf{M} is symmetric it is also positive-semidefinite and we may write its spectral decomposition as $\mathbf{M} = \mathbf{Q}_M\mathbf{\Lambda}_M\mathbf{Q}_M^\top$ where \mathbf{Q}_M is orthonormal.

To avoid that scaling of \mathbf{A} in $\mathbf{y} = \mathbf{A}\mathbf{x} + \mathbf{v}$ alters the impact of the disturbances \mathbf{v} we assume that its energy is normalized $\sum_{j=0}^{m-1} \sum_{k=0}^{n-1} \mathbf{A}_{j,k}^2 = n$, a constraint that is commonly written in terms of the Frobenius norm $\|\mathbf{A}\|_F^2 = n$. Whenever such a normalization is not explicit in the design flow we assume it to be applied as last step.

A. Optimizing Mutual Coherence

From the theory concerning mutual coherence, one is led to think that the lower the $\mu(\mathbf{B})$ the easier and better should be signal recovery. This is the common guideline of a plethora of methods that try to optimize \mathbf{A} so that \mathbf{B} has the least possible coherence thus adapting sensing to the signal sparsity dictionary.

Hardware-oriented adaptation techniques that are actually able to make the difference when coming to real-world implementations.

As a common starting point for all methods, note that, if the columns of \mathbf{B} are normalized to unit length, the very same definition of \mathbf{G} implies that $\mu(\mathbf{B})$ is the maximum of the magnitudes of the off-diagonal entries in \mathbf{G} . The prototype optimization problem that is being solved is

$$\min_{\mathbf{G} \in \mathfrak{G}, \mathbf{F} \in \mathfrak{F}} \|\mathbf{G} - \mathbf{F}\|_{\times} \quad (3)$$

where the $\|\cdot\|_{\times}$ norm can be either the sup norm $\|\cdot\|_{\infty}$ or the Frobenius norm $\|\cdot\|_F$ and the matrix set \mathfrak{F} is suitably defined in every variant of (3). As far as \mathfrak{G} is concerned, we need to limit the search to symmetric, positive semi-definite, low-rank matrices with a unit diagonal, i.e.,

$$\mathfrak{G} = \{\mathbf{G} \mid \mathbf{G}^T = \mathbf{G} \wedge \mathbf{G} \succeq 0 \wedge \text{rank}(\mathbf{G}) = m \wedge \text{diag}(\mathbf{G}) = \mathbf{1}\} \quad (4)$$

Since \mathbf{G} is symmetric, we have $\mathbf{G} = \mathbf{Q}_G \sqrt{\Lambda_G} \sqrt{\Lambda_G}^T \mathbf{Q}_G^T$. If Λ_G is the $m \times m$ upper left submatrix of Λ_G containing the m non-zero eigenvalues and \mathbf{Q}_G is the $d \times m$ submatrix of \mathbf{Q}_G containing the m leftmost columns, then we also have $\mathbf{G} = \mathbf{Q}_G \sqrt{\Lambda_G} \sqrt{\Lambda_G}^T (\mathbf{Q}_G)^T$ implying $\mathbf{B} = \sqrt{\Lambda_G}^T (\mathbf{Q}_G)^T$. With this, we may finally set $\mathbf{A} = \mathbf{B}\mathbf{D}^+$.

As far as \mathfrak{G} and \mathfrak{F} are convex sets defined as the intersection of elementary convex sets, the key technique for solving (3) is a mix of projected gradient descent [17] or shrinking in which the projection on \mathfrak{G} and \mathfrak{F} is computed by the method of alternating projections [18].

What follows is a brief overview of the proposals that use the above setting, each of them labeled with the prefix coh- followed by the initial of one of the proposing authors.

1) The “coh-S” Method in [19]

The method is equivalent to set $\|\cdot\|_{\times} = \|\cdot\|_F$ and $\mathfrak{F} = \{\mathbf{I}_d\}$, with \mathbf{I}_d the $d \times d$ identity matrix, thus simply pursuing the reduction of all off-diagonal entries of \mathbf{G} .

As noted in [20], pushing \mathbf{G} towards \mathbf{I}_d can be also interpreted, under suitable assumptions on the signal to acquire, in terms of minimization of the average squared error committed by an *oracle* estimator of ξ that knows in advance which are the non-zero entries.

2) The “coh-C” Method in [21]

The author notices that when $d > n$ the dictionary is redundant and this implies some coherence between the columns of \mathbf{D} . Since vectors forming a small angle get projected into vectors forming a small angle, such a coherence is imported in $\mathbf{A}\mathbf{D}$ whatever the \mathbf{A} .

Hence, instead of trying to reduce cross correlation, it is more sensible to make \mathbf{G} as close as possible to the Gram matrix of the dictionary alone $\mathbf{D}^T \mathbf{D}$. Hence, the method sets $\mathfrak{F} = \{\mathbf{D}^T \mathbf{D}\}$ and considers both $\|\cdot\|_{\times} = \|\cdot\|_F$ and $\|\cdot\|_{\times} = \|\cdot\|_{\infty}$.

3) The “coh-X” Method in [22]

The authors note that pushing \mathbf{G} towards \mathbf{I}_d is not completely justified by the objective of making the columns of \mathbf{B} as distinguishable as possible. In fact, assuming that *distinguishable* can be interpreted as *orthogonal*, a set of d vectors in \mathbb{R}^m that are *as orthogonal as possible* is a Grassmannian frame (GF) [23].

Then it would be convenient to define \mathfrak{F} as the set of all the possible Gram matrices corresponding to a GF. From [23] we know that, if all the columns are normalized to unit length, the absolute value of the scalar product of every pair of vectors in a GF matches μ_{\min} . Hence, the corresponding Gram matrix \mathbf{F} is such that $F_{j,k} = \pm \mu_{\min}$ for every $j \neq k$. Regrettably the set of such matrices is not convex and [22] relaxes it to one of its convex supersets. In particular it considers the set of symmetric, unit diagonal matrices, whose off-diagonal entries have a magnitude not larger than μ_{\min} , i.e., $\mathfrak{F} = \{\mathbf{F} \mid \mathbf{F}^T = \mathbf{F} \wedge \mathbf{F} \succeq 0 \wedge \text{diag}(\mathbf{F}) = \mathbf{1} \wedge |\mathbf{F}_{j,k}| \leq \mu_{\min} \forall j \neq k\}$.

4) The “coh-B” Method in [24]

This method puts an even stronger emphasis on frame-based design by considering Equiangular Tight Frames (ETFs) [25], [26]. Tightness means that $\|\mathbf{B}^T \mathbf{y}\|_2^2 = \alpha \|\mathbf{y}\|_2^2$ for some $\alpha > 0$. Equiangularity implies $\alpha = d/m$. Hence, the SVD of \mathbf{B} then becomes $\mathbf{B} = \mathbf{U}_B [\sqrt{d/m} \mathbf{I}_m \ \mathbf{0}] \mathbf{V}_B^T$ and this forces $\mathbf{G} = \mathbf{B}^T \mathbf{B}$ to have a well-defined spectral structure that is exploited to redefine \mathfrak{G} as

$$\mathfrak{G} = \left\{ \mathbf{G} \mid \mathbf{G} = \mathbf{Q}_G \begin{bmatrix} \frac{d}{m} \mathbf{I}_m & \mathbf{0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \mathbf{Q}_G^T \wedge \mathbf{Q}_G \in \mathbb{R}^{d \times d} \wedge \mathbf{Q}_G \mathbf{Q}_G^T = \mathbf{I}_d \right\}$$

where $\mathbf{Q}_G = \mathbf{V}_B$.

Further to that, [24] balances the goal of low mutual coherence with the need for minimizing the effect of non-perfect sparsity, something that we will not address in this overview.

5) The “coh-L” Method in [27]

This method mixes coh-S and coh-X. It first notices that, for a full-rank dictionary \mathbf{D} whose SVD features $\Lambda_D = [\Lambda \ \mathbf{0}]$ for some $n \times n$ diagonal and non-singular

matrix Λ , the solution of the optimization problem entailed by the coh-S method is $\mathbf{A} = [\mathbf{P}' \ \mathbf{0}] \mathbf{P}' \Lambda^{-1} \mathbf{U}_D^\top$ with $\mathbf{P}' \in \mathbb{R}^{m \times m}$ and $\mathbf{P}'' \in \mathbb{R}^{n \times n}$ arbitrary orthonormal matrices. The corresponding Gram matrix is

$$\mathbf{G} = \mathbf{V}_D \begin{bmatrix} \mathbf{P}'^\top & \mathbf{0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{I}_m & \mathbf{0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{P}' & \mathbf{0} \end{bmatrix} \mathbf{V}_D^\top$$

that can be further optimized according to coh-X using \mathbf{P}' as a degree of freedom.

6) The “coh-E” Method in [28]

As a slight variation, one may think that reducing *all* the pairwise correlations between columns of \mathbf{B} is a too ambitious goal. This method departs from such a worst-case target and concentrates on the largest correlations, replacing the merit figure in (3) with the average of the off-diagonal entries in \mathbf{G} that exceed a certain threshold t , i.e., $\sum_{|\mathbf{G}_{j,k}| \geq t} |\mathbf{G}_{j,k}| / \sum_{|\mathbf{G}_{j,k}| \geq t} 1$.

B. Adaptation Considering Second-Order Statistics

The common characteristic of the adaptation methods considered so far is that they rely on their design of \mathbf{A} starting from the knowledge of \mathbf{D} with algorithms metrics that do not consider how both signal and noise energy are processed by \mathbf{A} . Conversely, the adaptation methods we discuss in this section base their effectiveness on how such energy is processed in the encoder block. In particular, the last two methods we present use also the knowledge of the second-order statistical characterization of the input signals as an additional prior. Depending on the application, such knowledge could be either possessed in advance, or it must be obtained by estimation of the second-order statistics on a proper set of possible signals.

What follows is a brief overview of the corresponding proposals, each of them labeled with the prefix pow- followed by the initial of one of the proposing authors.

1) The “pow-C” Method in [20]

This method shares the attention to mutual coherence that characterizes coh-S and aims at obtaining \mathbf{G} as close as possible to \mathbf{I}_d . Yet, it notices that if two matrices \mathbf{A}' and \mathbf{A}'' exist such that setting $\mathbf{B}' = \mathbf{A}' \mathbf{D}$ and $\mathbf{B}'' = \mathbf{A}'' \mathbf{D}$ one has $\mathbf{B}'^\top \mathbf{B}' = \mathbf{B}''^\top \mathbf{B}'' = \mathbf{I}_d$, then, \mathbf{A}'' is preferable to \mathbf{A}' whenever $\|\mathbf{A}''\|_F < \|\mathbf{A}'\|_F$.

To see why, assume, for simplicity's sake, that the sparse representation of the signal is white, so that $\mathbf{E}[\xi \xi^\top] = \mathbf{I}_d$. The power of the signal-related components in the measurement vector $\mathbf{y} = \mathbf{B} \xi + \mathbf{v}$ is $\mathbf{E}[\|\mathbf{B} \xi\|_2^2] = \mathbf{E}[\xi^\top \mathbf{B}^\top \mathbf{B} \xi] = \text{tr}(\mathbf{B}^\top \mathbf{B} \mathbf{E}[\xi \xi^\top]) = \|\mathbf{B}\|_F^2$.

To enforce the energy constraint $\|\mathbf{A}\|_F^2 = n$ one sets $\mathbf{A} = (\sqrt{n}/\|\mathbf{A}'\|_F) \mathbf{A}'$ and thus $\mathbf{B} = (\sqrt{n}/\|\mathbf{A}'\|_F) \mathbf{B}'$ so that the power of the signal-related component is $(n/\|\mathbf{A}'\|_F^2) \|\mathbf{B}'\|_F^2 =$

$nd/\|\mathbf{A}'\|_F^2$ since the columns of \mathbf{B}' are normalized to unit length. Alternatively, by choosing \mathbf{A}'' instead of \mathbf{A}' one obtains that the power of the signal-related component becomes $(n/\|\mathbf{A}''\|_F^2) \|\mathbf{B}''\|_F^2 = nd/\|\mathbf{A}''\|_F^2 > nd/\|\mathbf{A}'\|_F^2$.

As the disturbance \mathbf{v} is independent of \mathbf{A} , increasing the signal-related component is surely beneficial and the method designs \mathbf{A} by solving

$$\min_{\mathbf{A} \in \mathbb{R}^{m \times n}} \|\mathbf{A}\|_F \quad \text{s.t.} \quad \mathbf{D}^\top \mathbf{A}^\top \mathbf{A} \mathbf{D} = \mathbf{I}_d \quad (5)$$

and then normalizing \mathbf{A} to satisfy the sensing energy constraint.

The solution of (5) can be written in terms of the SVD of \mathbf{D} and of the n -dimensional counter-diagonal unit matrix \mathbf{J}_n to set

$$\mathbf{A} = \mathbf{P} [\text{diag}(\lambda_{D_{m-1}}^{-1}, \lambda_{D_{m-2}}^{-1}, \dots, \lambda_{D_0}^{-1}) \ \mathbf{0}] \mathbf{J}_n \mathbf{U}_D$$

where \mathbf{P} is an arbitrary orthonormal matrix.

2) The “pow-P” Method in [29]

This method was devised for radar application. Here, dictionaries are typically built from the collection of responses from every possible target position and thus features a number of vectors d much larger than the number κ of non-null components in ξ , which correspond to the number of actual targets and is in the order of few units. It will show that this aspect also reflects to the fact that this method guarantees very high performance when d/k is very high while a strong performance degradation is observed for cases with lower d/k values. The general setting comprises a signal $\mathbf{D} \xi$, the disturbances \mathbf{v} and an interference contribution that we do not consider here. The optimization procedure for \mathbf{A} is heuristically derived by assuming that signal and noise are Gaussian with $\xi \sim \mathcal{N}(\mathbf{0}, \Sigma_\xi)$ for a certain covariance matrix Σ_ξ and $\mathbf{v} \sim \mathcal{N}(\mathbf{0}, \sigma^2 \mathbf{I}_n)$. Since $\mathbf{x} = \mathbf{D} \xi$ then one has $\mathbf{x} \sim \mathcal{N}(\mathbf{0}, \Sigma_x)$ with $\Sigma_x = \mathbf{D} \Sigma_\xi \mathbf{D}^\top$ that can be decomposed as $\Sigma_x = \mathbf{Q} \Sigma_x \Lambda \Sigma_x \mathbf{Q}^\top$.

With these assumptions, the method considers the estimation of ξ from \mathbf{y} and the corresponding confidence ellipsoid, i.e. the set in which estimations fall with a certain probability. In our case the shape and size of such an ellipsoid depend on the conditioned covariance $\Sigma_{\xi|\mathbf{y}}$. In particular, since the axes of the ellipsoid are proportional to the eigenvalues of $\Sigma_{\xi|\mathbf{y}}$ (that are non-negative), the method aims at making the distribution of estimations more concentrated, hopefully along the right direction, by minimizing

$$\min_{\mathbf{A} \in \mathbb{R}^{m \times n}} \text{tr} \left(\sum_{\xi|\mathbf{y}} \right) \quad \text{s.t.} \quad \begin{cases} \|\mathbf{A}\|_F^2 = n \\ \mathbf{A} \mathbf{A}^\top \text{ and } \sum_x \text{ have the same eigenvectors} \end{cases} \quad (6)$$

The solution of such a problem is given in terms of the eigenvalues of Σ_x and of the squared lengths t_k of the columns of $\Sigma_\xi \mathbf{D}^\top \mathbf{Q}_{\Sigma_x}$. More specifically, the method in [29] sets $\mathbf{A} = \text{diag}(\sqrt{\mu_0}, \dots, \sqrt{\mu_{m-1}}) \mathbf{Q}_{\Sigma_x, 0:m-1}$ where $\mathbf{Q}_{\Sigma_x, 0:m-1}$ is the matrix made of the first m columns of \mathbf{Q}_{Σ_x} and

$$\mu_j = \frac{t_j}{\lambda_{\Sigma_x j}} \frac{n + \sum_{k=0}^{L-1} \frac{\sigma}{\lambda_{\Sigma_x k}}}{\sum_{k=0}^{L-1} \frac{t_k}{\lambda_{\Sigma_x k}}} - \frac{\sigma}{\lambda_{\Sigma_x j}}$$

3) The “pow-R” Method in [30]

Real world signals are not white and this method aims at exploiting this prior. Non-whiteness depends on how average energy is distributed in the signal space. Such an information is contained in the correlation matrix $\mathbf{K}_x = \mathbf{E}[\mathbf{x}\mathbf{x}^\top]$ that is the starting point of this method. Consider \mathbf{K}_x and note that if \mathbf{x} were white, then all the eigenvalues of \mathbf{K}_x would be equal. Hence, one can measure non-whiteness with *localization* [31], that quantifies the deviation of the actual eigenvalues of \mathbf{K}_x from their equidistributed version

$$\mathcal{L}_x = \sum_{j=0}^{n-1} \left(\frac{\lambda_{\mathbf{K}_x j}}{\text{tr}(\mathbf{K}_x)} - \frac{1}{n} \right)^2 = \frac{\text{tr}(\mathbf{K}_x^2)}{\text{tr}^2(\mathbf{K}_x)} - \frac{1}{n} \quad (7)$$

Localization goes from 0 (white signals) to $1 - 1/n$ (signals whose energy concentrates along a single direction).

The method does not yield deterministic matrices \mathbf{A} . This slightly complicates the design flow but provides some advantages that can be exploited, for example, for effective implementations.

It assumes that \mathbf{A} is a random matrix made of independent and identically distributed non-white rows. If we indicate the generic row as \mathbf{a}^\top and the corresponding measurement with $y = \mathbf{a}^\top \mathbf{x}$, then the method aims at identifying rows with an high *rakeness*, i.e., with the ability of collecting the largest possible amount of energy from the signal and transfer it to the measurement³.

Since the power of the measurement is $\mathbf{E}[y^2] = \mathbf{E}[\mathbf{x}^\top \mathbf{a} \mathbf{a}^\top \mathbf{x}] = \text{tr}(\mathbf{K}_x \mathbf{K}_a)$ the natural design parameter is the correlation matrix $\mathbf{K}_a = \mathbf{E}[\mathbf{a} \mathbf{a}^\top]$ that is fixed by solving

$$\max_{\mathbf{K}_a \in \mathbb{R}^{n \times n}} \text{tr}(\mathbf{K}_x \mathbf{K}_a) \quad \text{s.t.} \quad \begin{cases} \mathbf{K}_a \succeq 0 \\ \mathbf{K}_a = \mathbf{K}_a^\top \\ \text{tr}(\mathbf{K}_a) = \frac{n}{m} \\ \mathcal{L}_a \leq \mathcal{L}_a^{\max} \end{cases} \quad (8)$$

where the first two constraints ensure that \mathbf{K}_a is a proper correlation matrix, and the trace constraint makes the

³This is similar to what some of the authors employed in (chaos-based) DS-CDMA communication, where chip waveforms, spreading sequence statistics and rake receivers taps were jointly selected to collect (rake) as much energy as possible at the received side [32], [33]. In other words, the underlying idea behind the rakeness-based CS is to adapt the statistics of the sensing sequences to the class of input signals by exploiting the fact that the energy and thus the information content of the signal is not uniformly distributed over its whole domain.

power of each row equal to n/m so that the m -rows matrix \mathbf{A} satisfies the sensing energy constraint $\|\mathbf{A}\|_F = n$ on average.

The localization constraint is used to control the amount of adaptation of the sensing matrix. When $\mathcal{L}_a^{\max} = 0$ then the rows are forced to be white and there is no adaptation. When $\mathcal{L}_a^{\max} = 1 - 1/n$ all the rows come up lying along the principal component of \mathbf{K}_x thus making all the measurements maximally energetic but indistinguishable and thus useless.

The problem in (8) can be given an analytical solution that, under the assumption $\mathcal{L}_a^{\max} \leq \mathcal{L}_x$, reads

$$\mathbf{K}_a = \frac{n}{m} \frac{\mathbf{K}_x}{\text{tr}(\mathbf{K}_x)} \sqrt{\frac{\mathcal{L}_a^{\max}}{\mathcal{L}_x}} + \frac{1}{m} \mathbf{I}_n \left(1 - \sqrt{\frac{\mathcal{L}_a^{\max}}{\mathcal{L}_x}} \right)$$

Once that \mathbf{K}_a is fixed, one may draw $\mathbf{a}' \sim \mathcal{N}(0, \mathbf{I}_n)$ and set $\mathbf{a} = \mathbf{Q}_{\mathbf{K}_a} \sqrt{\Lambda_{\mathbf{K}_a}} \mathbf{a}'$ to produce a Gaussian row \mathbf{a}^\top with the proper correlation.

Further to that, methods exist [34], [35] to reproduce the same statistical behavior even if the entries of \mathbf{A} are constrained to some low-cardinality, hardware-friendly [36], [37], set of values like $\mathbf{A}_{j,k} \in \{-1, 1\}$, $\mathbf{A}_{j,k} \in \{-1, 0, 1\}$, or $\mathbf{A}_{j,k} \in \{0, 1\}$. If hardware friendliness is a major issue, the constraint on the kind of entries in \mathbf{A} can be plugged directly into the rakeness-based design flow by adjusting (8) [31] to yield sensing matrices that allow substantial savings in computational complexity.

C. Power-Based Adaptation is not Only About Noise

The most obvious rationale beyond pow-C and pow-R methods is that they increase the power of the signal-related component $\mathbf{A}\mathbf{x}$ in $\mathbf{y} = \mathbf{A}\mathbf{x} + \mathbf{v}$ thus countering the effect of noise. Yet, there is a deeper reason regulating their effectiveness that can be illustrated

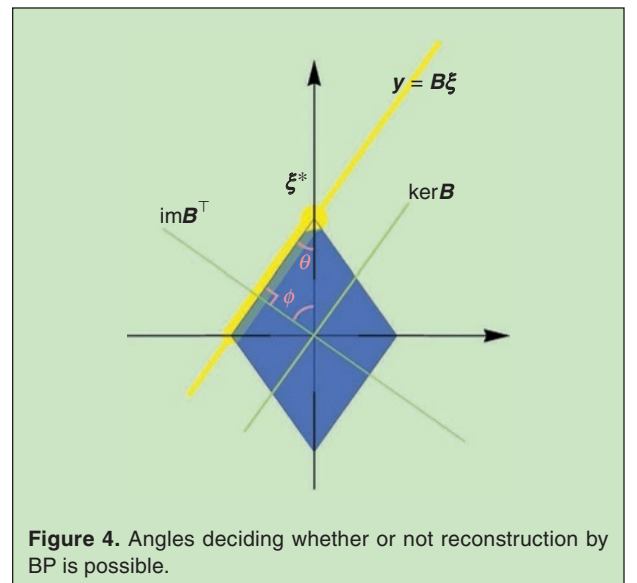


Figure 4. Angles deciding whether or not reconstruction by BP is possible.

using the polytope interpretation of CS when \mathbf{D} is an orthonormal basis.

To illustrate the core concept rotate Figures 3-(b) until it appears as Figure 4. From this point of view, it is clear that BP is not effective as the angle θ between $\ker \mathbf{B}$ and the signal ξ^* is equal to the angle between the sparse representation of the signal itself and a facet of the cross-polytope.

To generalize such an unfavorable condition, indicate with $A(\xi^*)$ the union of the facets that are adjacent to ξ^* . As an example, in Figure 3, $A(\xi^*)$ is made of the four segments (1-dimensional facets) and the 4 triangles (2-dimensional facets) on the surface of the blue cross-polytope that have ξ^* as a vertex. Based on $A(\xi^*)$, define the set $\Theta(\xi^*)$ of the angles formed by the sparse representation of the signal with any segment

having ξ^* as a vertex and lying on $A(\xi^*)$. Problems arise when the angle θ between $\ker \mathbf{B}$ and ξ^* belongs to $\Theta(\xi^*)$.

To prevent this from happening, we may choose a \mathbf{B} such that the angle θ is larger than $\max \Theta(\xi^*)$. Since $\text{im } \mathbf{B}^\top$ is orthogonal to $\ker \mathbf{B}$ this translates into the requirement that the angle ϕ between the rows of \mathbf{B} (whose linear combinations yield $\text{im } \mathbf{B}^\top$) and ξ^* is smaller than $\pi/2 - \max \Theta(\xi^*)$. If \mathbf{D} is orthonormal, the angles between the rows of \mathbf{B} and ξ^* are the same as those between the rows of $\mathbf{B}\mathbf{D}^\top = \mathbf{A}$ and $\mathbf{D}\xi^* = \mathbf{x}^*$.

Finally, given \mathbf{x}^* and assuming that the rows of \mathbf{A} are normalized to the same length, reducing the angle means increasing the magnitude of each entry of $\mathbf{y} = \mathbf{A}\mathbf{x}$, i.e., its energy.

IV. Encoder Adaptation at Work

We test the above methods in a common environment with $n = 128$ and in which \mathbf{D} is either a random orthonormal matrix or a random dictionary with $d = 256$ and normalized columns. Sparsity is set to $\kappa = 6$.

Each signal window is generated starting from a random vector $\mathbf{x}' \sim \mathcal{N}(\mathbf{0}, \Sigma_{\mathbf{x}'})$ for a certain $\Sigma_{\mathbf{x}'}$. Such a vector is then decomposed along \mathbf{D} by setting $\xi' = \arg \min_{\xi \in \mathbb{R}^d} \|\xi\|_1$ s.t. $\mathbf{x}' = \mathbf{D}\xi'$. The vector ξ' is then sparsified into the vector ξ'' by keeping only the κ largest components while setting the others to 0. The signal is finally generated as $\mathbf{x} = \mathbf{D}\xi''$. The matrix $\Sigma_{\mathbf{x}'}$ is chosen to make \mathbf{x} slightly low-pass and $\mathcal{L}_{\mathbf{x}} \simeq 0.03$ of the same magnitude of some classical real-world signals.

Whatever method is used to build the matrix \mathbf{A} , we compute the measurement vector $\mathbf{y} = \mathbf{A}\mathbf{x} + \mathbf{v}$ with $\mathbf{v} \sim \mathcal{N}(\mathbf{0}, 10^{-6} \mathbf{I}_m)$ and go from \mathbf{y} to an estimation $\hat{\mathbf{x}}$ of \mathbf{x} by means of BPDN as implemented in [38].

We evaluate the quality of reconstruction with the Reconstruction Signal-to-Noise-Ratio (RSNR) $\|\mathbf{x}\|_2^2 / \|\mathbf{x} - \hat{\mathbf{x}}\|_2^2$. Performance is assessed by considering 4000 Montecarlo trials and computing the average RSNR that we indicate with ARSNR. Though average performance is not a complete characterization of the effectiveness of CS it will suffice here to give a general idea of what can be obtained by adaptation.

As a reference case we assume the one in which the entries of \mathbf{A} , before energy normalization, are independent normals $\mathcal{N}(0, 1)$. It is a classical setting that we label as “i.i.d.” and allows to quantify the improvements due to different adaptation policies⁴

Since hardware implementations greatly benefit from constraining the $\mathbf{A}_{j,k}$ to a small number of possible values, we also consider, as a second setting, the option of

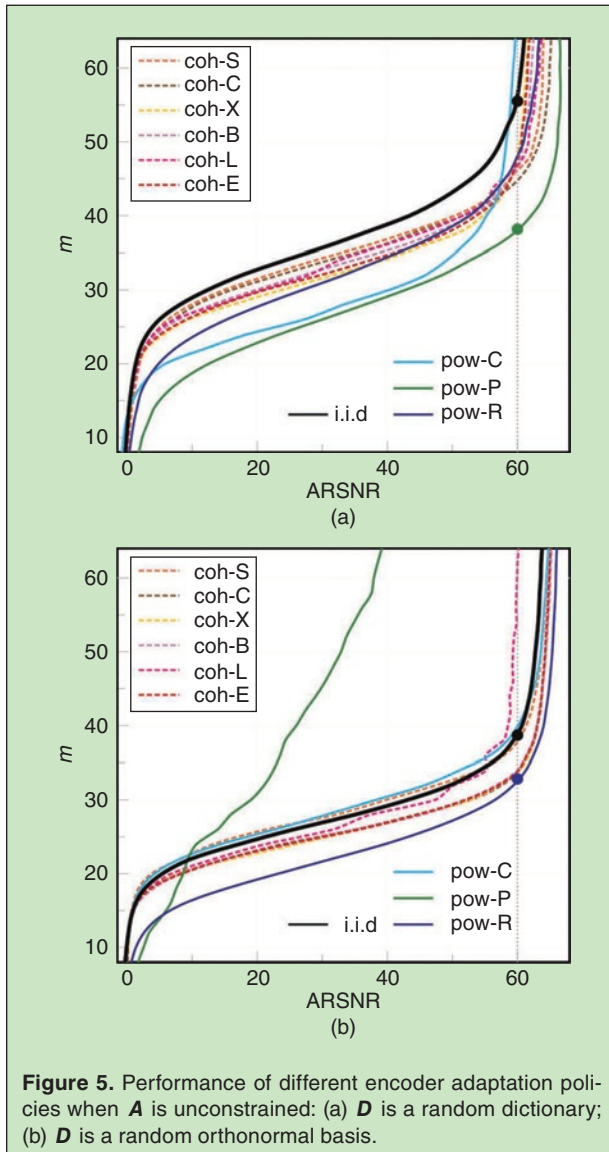


Figure 5. Performance of different encoder adaptation policies when \mathbf{A} is unconstrained: (a) \mathbf{D} is a random dictionary; (b) \mathbf{D} is a random orthonormal basis.

⁴The MATLAB code used to obtain these results is available at <https://goo.gl/6hknan>.

substituting $\mathbf{A}_{j,k}$ with $m^{-1/2} \text{sign}(\mathbf{A}_{j,k})$ to obtain antipodal adapted matrices.

Figure 5 and Figure 6 plot the number of measurements against the ARSNR that they allow to achieve. Since $n = 128$, the vertical span is limited to $m \leq n/2 = 64$ to zoom in the area in which the compression rate is at least 2:1. From the shape of all the curves in the figures it is clear that performance tends to saturate when $m > 64$.

In all plots, the i.i.d. reference case is the black line. Plots are from the designer's point of view: one chooses the reconstruction quality along the horizontal axis and finds the minimum number of measurements (and thus the compression ratio) needed to obtain it. Hence, the lower the curve, the better the method in exploiting the features of the signal to optimize CS performance.

Note that the methods behave differently in the dictionary and orthonormal basis cases. In particular, it is very interesting to notice that the best option in the dictionary case (pow-P), yields extremely low performance in the basis case, in which pow-R consistently delivers the best performance.

It is also to notice that coherence-based methods (dashed lines) seem to provide smaller improvements with respect to power-based methods (solid lines) and to suffer more from antipodal quantization passing from Figure 5 to Figure 6. On the contrary, antipodal quantization does not cause any severe loss in performance to the i.i.d. reference case and to the power-based method.

Overall, adaptation proves to be quite effective. As an example, consider a target ARSNR of 60 dB for a dictionary-based CS. In both unconstrained or antipodal \mathbf{A} cases, non-adapted CS needs $m^{\text{i.i.d.}} = 57$ measurements for a 2.2:1 compression ratio. The pow-P method reduces it to $m^{\text{pow-P}} = 38$ for unconstrained \mathbf{A} and $m^{\text{pow-P}} = 40$ for antipodal \mathbf{A} thus yielding compression ratios of 3.4:1 and 3.2:1 respectively.

In the basis case, non-adapted CS needs $m^{\text{i.i.d.}} = 39$ measurements for a 3.3:1 compression ratio. Yet, the pow-R method yields $m^{\text{pow-R}} = 32$ in both the unconstrained and antipodal \mathbf{A} cases, thus bringing compression ratio to 4:1.

V. Adaptation at the Decoder Side

Though, in principle, any convex optimization solver can be used to solve BPDN, there is a flourishing literature developing alternative reconstruction algorithms. For example, instead of depending on the $\|\cdot\|_1$ norm and its favorable geometry, signal reconstruction can be approached from completely different points of view, e.g., from the estimation, or machine learning, or regression point of view [39]–[41]. Moreover, procedures exist that retrieve the original signal by generating solutions to

$\mathbf{y} = \mathbf{B}\xi$ iteratively and adjusting their sparsity at each step. Different heuristics may be used to promote sparsity and this gives rise to different methods [5]–[7]. The simple structure of these methods, and their good performance, make them ideal for CS embodiments in which the resources devoted to signal reconstruction are limited. As an example, the approach of Orthogonal Matching Pursuit (OMP) tries to reconstruct $\text{supp}(\xi) = \{j | \xi_j \neq 0\}$ iteratively by looking for the columns of \mathbf{B} that have the highest correlation with the measurements vector \mathbf{y} , a simplified pseudo-code being in Table I.

Among this abundance, few methods concentrate on adapting the decoding procedure to the features of the signal. Since the task of the decoder is to retrieve the sparse representation ξ , it is most natural to exploit priors applying to that space.

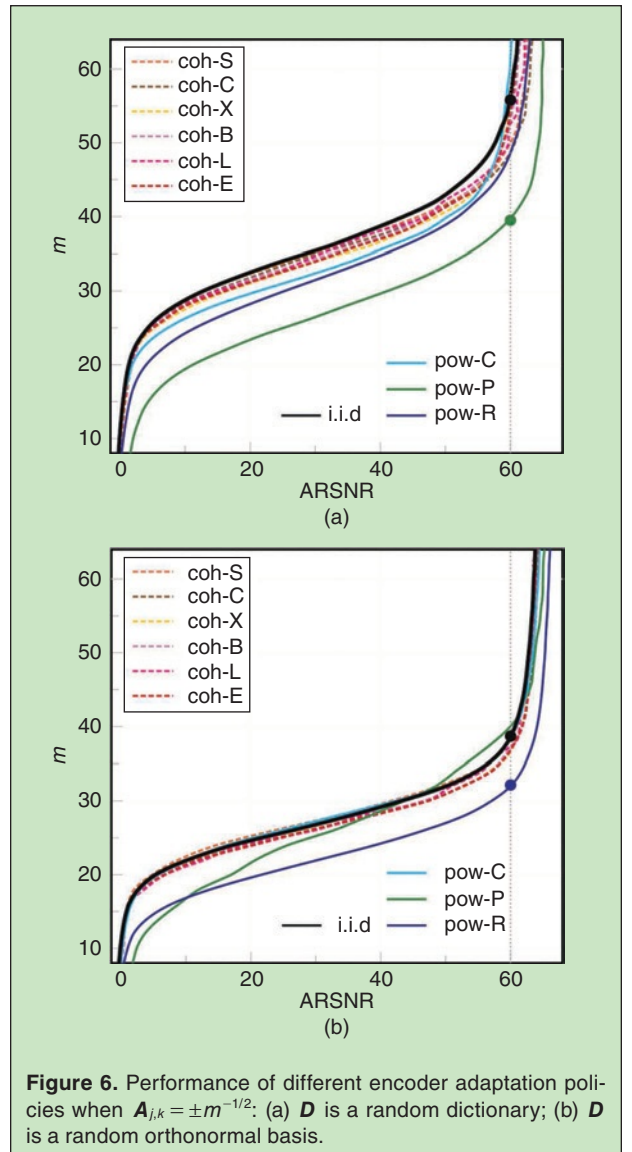


Figure 6. Performance of different encoder adaptation policies when $\mathbf{A}_{j,k} = \pm m^{-1/2}$: (a) \mathbf{D} is a random dictionary; (b) \mathbf{D} is a random orthonormal basis.

In particular, the priors we consider concern $\text{supp}(\xi) = \{j | \xi_j \neq 0\}$, i.e., the positions of the non-zero elements in ξ , or the magnitudes of the non-zero elements in ξ .

1) The “dec-ZZ” Method in [8]

This approach assumes that the signal is not only sparse but also *block-sparse*. Blocks are subvectors $\xi^{[j]}$ of ξ containing adjacent entries so that one may partition ξ in β blocks $\xi^\top = [\xi^{[0]\top} \dots \xi^{[\beta-1]\top}]$. The signal is block-sparse if $\text{supp}(\xi)$ is always contained in the union of a number of blocks $\ll \beta$.

Block-sparsity is a stronger prior than simple sparsity [42] and can be paired with Bayesian learning [8] to yield effective reconstruction algorithms. The core idea is to assume that each block follows a parameterized multivariate Gaussian distribution $\xi^{[j]} \sim \mathcal{N}(0, \gamma_j \Sigma_{\xi^{[j]}})$ and is independent of the other blocks so that $\xi_j \sim \mathcal{N}(0, \Sigma_\xi)$ with $\Sigma_\xi = \text{diag}(\gamma_0 \Sigma_{\xi^{[0]}}, \dots, \gamma_{\beta-1} \Sigma_{\xi^{[\beta-1]}})$. With this model, $\gamma_j = 0$ implies that the block does not cover $\text{supp}(\xi)$ and thus controls the block sparsity.

Decoding is then divided in two steps. In the first step the parameters γ_j and $\Sigma_{\xi^{[j]}}$ are *learnt* for $j = 0, \dots, \beta - 1$. In the second step they are used to decode ξ by means of straightforward Maximum-A-Posteriori estimation

$$\hat{\xi} = \sum_{\xi} \mathbf{B}^\top \left(\sigma^2 \mathbf{I}_m + \mathbf{B} \sum_{\xi} \mathbf{B}^\top \right)^{-1} \mathbf{y}$$

Depending on the different strategies for learning the γ_j and $\Sigma_{\xi^{[j]}}$, this approach gives rise to different methods that differ in computational complexity more than in final performance.

2) The “dec-JZ” Method in [43]

In this case one assumes that, when $\xi_j \neq 0$ then its average magnitude varies with j . This is most natural when,

for example, \mathbf{D} is a wavelet-like orthonormal basis that decomposes the signal into a sequence of *approximation/detail* pairs whose typical decay is known by design of can be identified.

This decay information can be plugged into BPDN by altering the sparsity promoting norm from $\|\xi\|_1$ to $\|\mathbf{W}^{-1}\xi\|_1$ where \mathbf{W} is the diagonal matrix aligning the coefficients modeling the decay.

The method appears to be most effective when BPDN is solved considering its *lasso* relaxation, i.e., in

$$\min_{\xi \in \mathbb{R}^d} (1 - \alpha) \|\mathbf{W}^{-1}\xi\|_1 + \alpha \|\mathbf{y} - \mathbf{B}\xi\|_2^2$$

where the parameter α administers the weight of the two components in the relaxation.

3) The “dec-P” Method in [9], [44]

In OMP, the new columns of \mathbf{B} to be inserted in the set that is deemed to be necessary to reproduce the measurements are selected for their alignment with the residual measurement. A prior of the kind used in the previous method can alter this selection by altering the opportunity of choosing a column depending on the decay coefficient of the corresponding entry in ξ .

This can be done by changing Line 5: in Table I with $j = \text{argmax}_k |B_{:,k}^\top [(1 - \alpha)\mathbf{W}^{-1} + \alpha \mathbf{I}_d] \Delta \mathbf{y}|$, where the parameter α administers the trade-off between following the correct decay and aligning with the residual.

VI. Back to ECGs

The ECG signals we mentioned in the introduction offer the opportunity of testing the effect of adaptation at both the encoder and decoder side. In fact, they can be given an approximately sparse representation along, for example, a Daubechies-6 wavelet basis \mathbf{D} that has a dyadic scaling and thus induces a blockwise halving decay in the typical magnitude of the coefficients.

We consider windows containing $n = 512$ samples taken at 360 sample/s from a classical procedure generating clean and realistic ECG tracks [45] and superimpose a noise vector $\nu \sim \mathcal{N}(\mathbf{0}, 10^{-6} \mathbf{I}_m)$ to the measurement vector \mathbf{y} .

Figure 7 compares the performance of the three above decoding strategies against non-adapted BPDN. In all cases \mathbf{A} is made of independent Gaussian random variables. Though with different profiles, all methods give definite advantages over non-adapted BPDN.

With reference to the hearth monitoring device briefly sketched in the introduction, we may also evaluate what could be the overall impact of adaptation both at the encoder and decoder side.

Since we are dealing with a portable device in which the resources for the computation of \mathbf{y} are limited, we constrain $\mathbf{A} = \pm m^{-1/2}$.

Table I.
Pseudo-code of OMP.

- 1: $\zeta \leftarrow []$ \triangleright initialize the vector that will contain the non-zero components of $\hat{\xi}$
- 2: $J \leftarrow []$ \triangleright initialize the vector that will contain $\text{supp}(\hat{\xi})$
- 3: **repeat**
- 4: $\Delta \mathbf{y} \leftarrow \mathbf{y} - \mathbf{B}_{:,J} \zeta$ $\triangleright \mathbf{B}_{:,J}$ is the submatrix of \mathbf{B} with columns indexed by J
- 5: $j = \text{argmax}_k |B_{:,k}^\top \Delta \mathbf{y}|$ \triangleright column $B_{:,k}$ of \mathbf{B} that best matches the measurements residual
- 6: $J \leftarrow [J \ j]$ \triangleright include it in J
- 7: $\zeta \leftarrow \mathbf{B}_{:,J}^+ \mathbf{y}$ \triangleright re-estimate ζ by pseudo-inversion
- 8: **until** convergence
- 9: $\hat{\xi}_j \leftarrow \begin{cases} \zeta_k & \text{if } j = J_k \\ 0 & \text{otherwise} \end{cases}$ \triangleright put non-zero components back into $\hat{\xi}$

The previous analysis (see Figure 6(b)) suggests that, since \mathbf{D} is an orthonormal basis, it is convenient to use the pow-R method that yields consistent improvement across multiple target quality levels. From [12] we get that LQ reconstruction supporting, for example, heart rate estimation may feature an ARSNR as low as 7 dB. Yet, from [46] we get that HQ reconstruction must provide an ARSNR not smaller than 34 dB.

From Figure 7 we get that, when neither the encoder nor the decoder is adapted, an LQ recovery of the signal requires $m^{\text{LQ}} = 86$ thus yielding a 6.0:1 compression, while HQ recovery requires $m^{\text{HQ}} = 232$ thus yielding a 2.2:1 compression. This second result is a pretty standard one as it is accepted that straightforward CS applied to ECGs is a computationally effective way of enjoying a compression in the order of 2:1.

Furthermore, introducing pow-R at the encoder and dec-P at the decoder, i.e., the case where both encoder and decoder are designed in according to an adapted CS method, the number of measurements is reduced to $m^{\text{LQ}} = 36$ and $m^{\text{HQ}} = 137$ thus increasing the compression ratio from 6.0:1 to 14.2:1 in the LQ case and from 2.2:1 to 3.7:1 in the HQ case. To give an intuitive feeling on the improvement due to adaptation we may consider 5 windows of an ideal ECG profile as reported at the top of Figure 8. Based on that profile we test both the non-adapted encoder-decoder pair and the adapted one, using the number of measurements that make the adapted pair work either at LQ ($m^{\text{LQ}} = 36$) or HQ ($m^{\text{HQ}} = 137$).

In Figure 8, the yellow-background plots refer to the $m^{\text{LQ}} = 36$, while the green-background plots refer to $m^{\text{HQ}} = 137$. Independently of the compression, adapted CS widely outperforms the non-adapted option.

VII. Adaptation for Hardware Implementation

When dealing with implementations of CS-based acquisition systems, the concept of *adaptation* can be considered also from an “hardware-oriented” perspective. As an example, CS has been characterized so far by the set of linear projections expressed by $\mathbf{y} = \mathbf{Ax}$. However, when dealing with a real world input signal, the very concept of projection and scalar product is heavily dependent on the way in which the input signal information is encoded. In other word, it is fundamental to keep into account the *signal representation*.

The aim of this section is to review both standard and innovative approaches to examine practical problems that can arise in hardware implementations of CS-based acquisition systems and present an overview of solutions employed in integrated circuits presented so far in the literature. Referring to the above example, a brief survey is enough to identify the many different

possibilities in which the linear projections $\mathbf{y} = \mathbf{Ax}$ are computed according to the different input signal model. The solution for this and other issues usually requires the adaptation of the CS framework either at circuitual or even at system level.

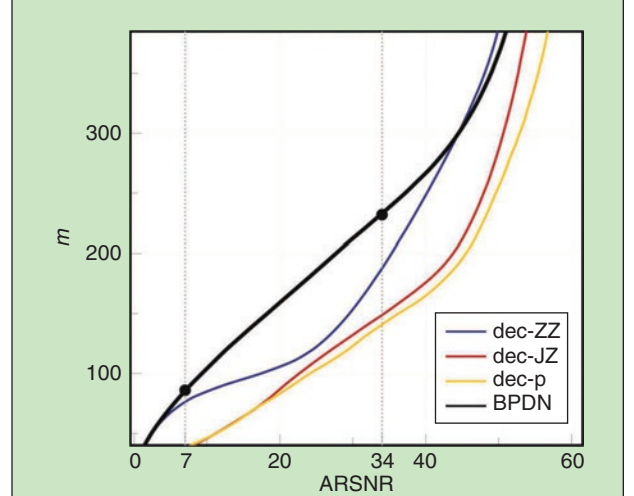


Figure 7. Performance of different decoder adaptation policies.

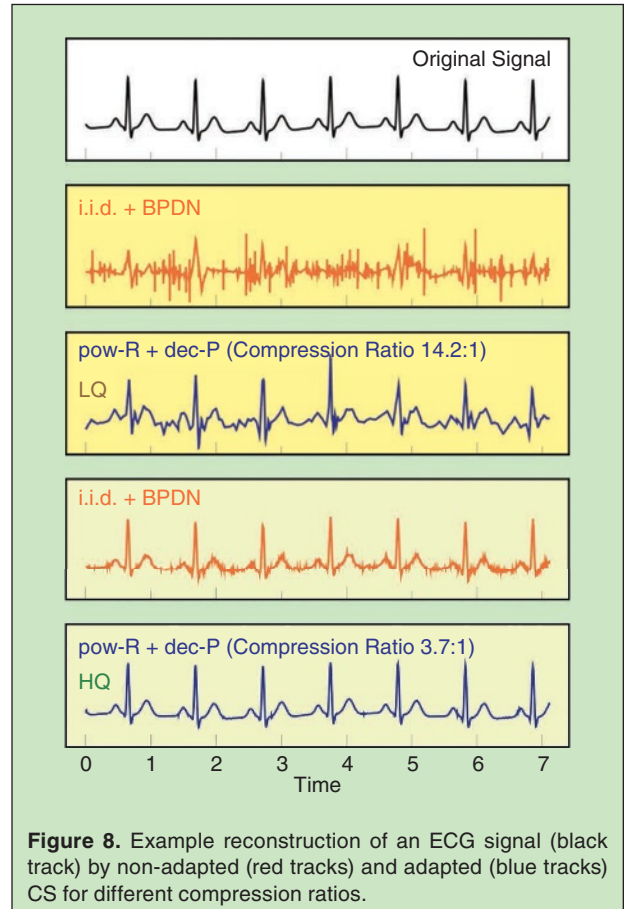


Figure 8. Example reconstruction of an ECG signal (black track) by non-adapted (red tracks) and adapted (blue tracks) CS for different compression ratios.

Regrettably, a rapid scan of the recent literature on CS related works reveals that among the overwhelming number of works that can be found, only a negligible fraction of them deals with the actual circuitual implementation of the proposed algorithm or technique.

To the best of authors' knowledge, the first prototype capable of implementing a CS-based system via the generic $\mathbf{y} = \mathbf{A}\mathbf{x}$ product has been presented in [47]. The circuit is a sub-Nyquist rate receiver for radar pulse signal designed in 90 nm technology, capable to acquire signals up to 2 GHz. In [48], the authors describe a CS-based data acquisition front-end for a radio frequency (RF) communication system implemented in 90 nm CMOS process. The work in [49] presents an analog front-end for ECG signals designed in 180 nm CMOS process, while [50] reports an area and power efficient multi-electrode arrays acquisition system based on CS designed in 180 nm CMOS process, outperforming previously presented works in terms of compression rate and reconstruction quality by a run-time adaptation. The work [51] describes a low-power sub-Nyquist sampler for the multichannel acquisition of cortical intracranial electroencephalographic (iEEG) signals. The peculiarity of this architecture, which has been fabricated in 180 nm CMOS process, is to consider the signal features not only in the temporal domain, but also in the spatial domain. The architecture presented in [37], designed in 180 nm CMOS process, is an analog-to-information converter for generic biomedical signals. It introduces a smart saturation checking mechanism with which it is possible to reconstruct the acquired signal even if many measurements suffer saturation, and exploits the aforementioned pow-R approach introduced in Section III-B. In [52], the authors propose a run-time signal evaluation module (indicated as *dynamic knob*) designed in 130 nm CMOS process, with the aim of improving the quality of the following CS encoder by adapting a few parameters towards the input biosignal dynamics. Finally, in [53], the complexity of the VLSI implementation of the generator of the sensing matrix \mathbf{A} is investigated, and the hardware efficient generation of deterministic sparse sensing matrices is considered.

A. Computation of Compressed Measurements

All aforementioned implementations share the same philosophy: in order to compute m different measurements, the very same hardware block is either replicated m times or used in an interleaved way m times, and driven by the input signal \mathbf{x} and the m different instances corresponding to the rows of \mathbf{A} . For the sake of simplicity, in the following we will focus on the scalar product $y = \mathbf{a}^\top \mathbf{x}$, where \mathbf{a} is a generic row of \mathbf{A} and y the corresponding element of the measurement vector.

A first group of works [37], [47]–[49], [51], [54] deal with an *analog* input signal represented as a function $x(t)$ of the time variable t . As an example, $x(t)$ may be the output of a sensor (typically a voltage), or, more frequently, $x(t)$ is differentially encoded, i.e., it is represented as the difference between two (voltage) quantities as $x(t) = x^+(t) - x^-(t)$. In a few cases, as in [51], the authors consider a multi-channel scenario, and the input signal $\mathbf{x}(t)$ is actually an array of p signals coming from different sensors.

For the sake of simplicity, in the following we limit ourselves to the scalar case regardless of the fact that the actual implementation of x is differential or single-ended.

When dealing with an analog signal, two issues immediately arise if one thinks about the computation of $y = \mathbf{a}^\top \mathbf{x}$: *i*) according to the standard CS model, \mathbf{x} is assumed to be a vector, while in a real implementation the best fit for the input signal is a function of time $x(t)$; *ii*) \mathbf{x} is n -dimensional, while $x(t)$ is defined over the whole \mathbb{R} , i.e., it has an infinite dimensionality.

The standard solutions adopted to reconcile the different signal models are sketched in Figure 9. The common way to cope with dimensionality is by *windowing* $x(t)$ [37], [47]–[49]. The input signal is sliced to get the functions $x^{(l)}(t)$, $x^{(l+1)}(t)$, $x^{(l+2)}(t)$, ..., each of them defined on contiguous and non overlapping time intervals $I^{(l)}$, $I^{(l+1)}$, $I^{(l+2)}$, ..., and such that $x^{(l)}: I^{(l)} \mapsto \mathbb{R}$. The l -th slice of the input signal $x^{(l)}(t)$ gives rise to measurements $\mathbf{y}^{(l)}$, that are used to reconstruct $x^{(l)}(t)$. The complete input signal can then be achieved by joining all the reconstructed slices.

Conversely, coping with the first issue has not a unique solution. The most general approach is that adopted by [47], [48], where the generic measurement y is achieved by a continuous time *multiply-and-integrate* architecture as in the “analog continuous-time” case of Figure 9. The l -th slice of the input signal $x^{(l)}(t)$ is first multiplied by a sensing function $a(t)$ (assumed defined over $I^{(l)}$) and then integrated over $I^{(l)}$. Focusing for simplicity on the case $l = 0$ where $I^{(0)} = [0, T_w]$, the measurement is expressed as

$$y^{(0)} = \int_0^{T_w} a(t)x^{(0)}(t)dt \quad (9)$$

It is interesting to notice that also this case can be easily incorporated into the standard framework $y = \mathbf{a}^\top \mathbf{x}$ under the reasonable assumption that $a(t)$ is generated starting from n coefficients \mathbf{a}_k stored into a local memory as the pulse-amplitude modulated (PAM) function $a(t) = \sum_{k=0}^{n-1} \mathbf{a}_k g(t \cdot n/T_w - k)$, being $g(\cdot)$ a normalized pulse⁵.

⁵A typically, but not necessary, choice for $g(\cdot)$ is the rectangular pulse.

By replacing the definition of $a(t)$ in (9), we get

$$\begin{aligned} y &= \sum_{k=0}^{n-1} \mathbf{a}_k \int_0^{T_w} g\left(t \frac{n}{T_w} - k\right) x^{(0)}(t) dt \\ &= \sum_{k=0}^{n-1} \mathbf{a}_k \tilde{\mathbf{x}}_k^{(0)} = \mathbf{a}^\top \tilde{\mathbf{x}}^{(0)} \end{aligned}$$

where we have implicitly defined a generalized Nyquist-rate samples vector $\tilde{\mathbf{x}}^{(0)} = [\tilde{x}_0^{(0)}, \tilde{x}_1^{(0)}, \dots, \tilde{x}_{n-1}^{(0)}]$ where samples are taken at Nyquist rate but their amplitude is related to

$$\hat{\mathbf{x}}_k^{(0)} = \int_0^{T_w} g\left(t \frac{n}{T_w} - k\right) x^{(0)}(t) dt$$

Note that, in many practical cases, $\tilde{\mathbf{x}}$ is not so different from the Nyquist rate sample vector \mathbf{x} . In fact, we have $\tilde{\mathbf{x}} = \mathbf{x}$ when $g(\tau)$ is the standard Dirac delta operator $\delta(\tau)$. Yet, in practical implementations, it is common to replace $\delta(\tau)$ with a normalized pulse equal to the ideal rectangular pulse $\chi(\tau) = 1$ when $0 \leq \tau < 1$, and $\chi(\tau) = 0$ elsewhere. In this case the generalized coefficient vector can be considered a good approximation of Nyquist-rate sample vector, i.e., $\tilde{\mathbf{x}} \approx \mathbf{x}$ if the input signal is quasi-stationary. Note also that the CS

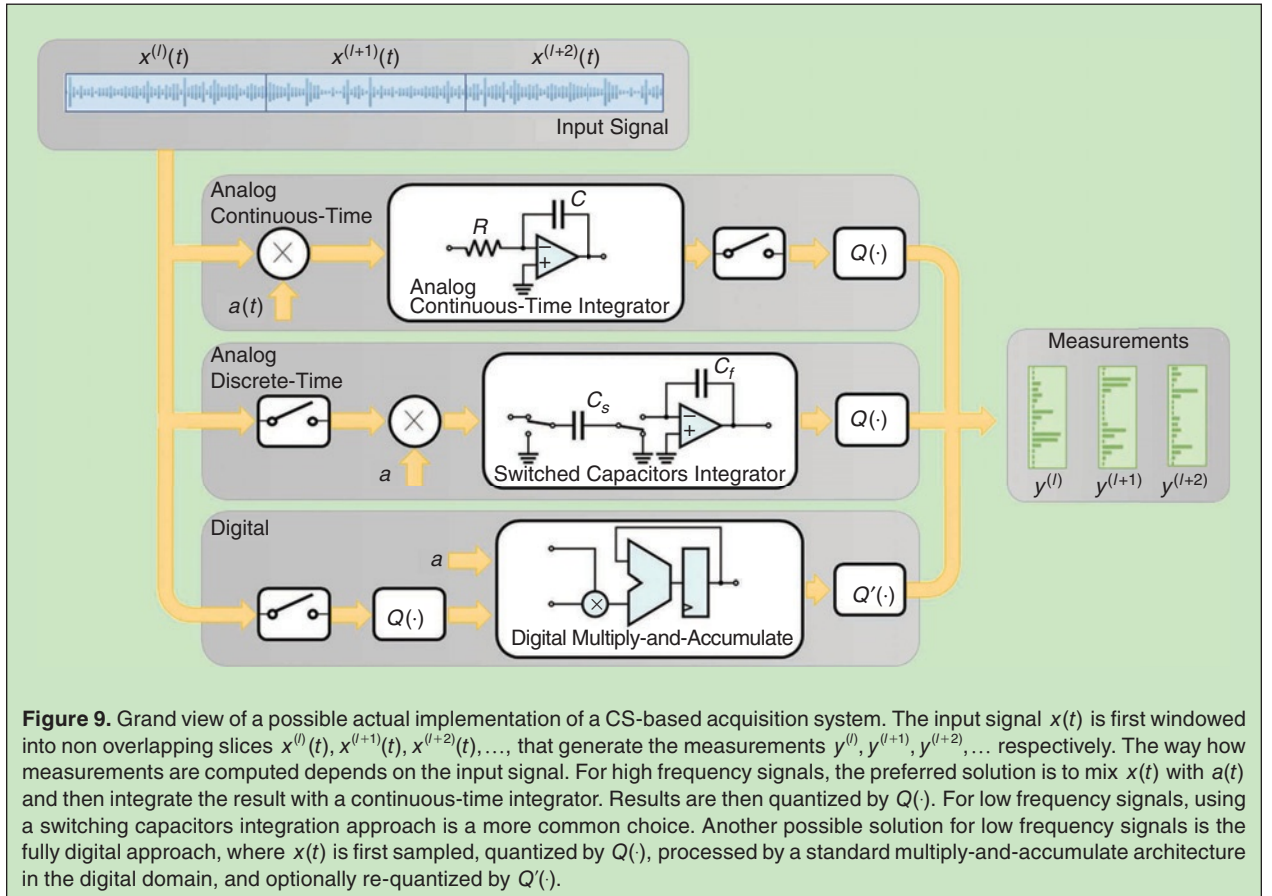
reconstruction procedure will retrieve the generalized sample vector $\tilde{\mathbf{x}}$.

Moreover, if the input signal is low frequency, different approaches are possible. A solution adopted in [37], [49], [51] is to consider a switched capacitor architecture. In this case, we are dealing with a *discrete-time* input signal model thanks to the intrinsic sampling capabilities guaranteed by this class of circuits. The generic l -th time windows of length T_w , defined in the interval $I^{(l)}$ is sampled at rate n/T_w to generate a n -length analog samples vector. Focusing, for the sake of simplicity, on $I^{(0)} = [0, T_w]$, we get

$$\mathbf{x}^{(0)} = \left[x^{(0)}(0), x^{(0)}\left(\frac{T_w}{n}\right), \dots, x^{(0)}\left((n-1)\frac{T_w}{n}\right) \right]^\top$$

The Nyquist samples of the input signal are then processed with a standard *multiply-and-accumulate* (MAC) analog architecture, shown in the “analog discrete-time” case of Figure 9, where a clock signal is assumed whose period is divided into two phases.

In the first one, each sample of $\mathbf{x}_k^{(0)} = x^{(0)}(kT_w/n)$ is multiplied by \mathbf{a}_k , and the results sampled by the C_s . In the second phase, all the charge stored in C_s is transferred to the feedback capacitor C_f , that accumulates



Adaptation proves to be a tool that should be mastered in practical applications to unleash the full potential of compressed sensing.

the voltage level to be provided as circuit output. After n integration time steps, and assuming $C_s = C_I$, we get at the circuit output

$$\sum_{k=0}^{n-1} \mathbf{a}_k \mathbf{x}_k^{(0)} = \mathbf{a}^\top \mathbf{x}^{(0)} = y^{(0)}$$

that is the measurement associated to the generic row \mathbf{a}^\top for the time windows I^0 .

As final step, in both the considered cases (i.e., when $x(t)$ is high-frequency and measurements are computed by means of a continuous-time integrator [47], [48], and when $x(t)$ is low-frequency and measurements are achieved with a switched capacitor integrator [37], [49], [51]) y is finally converted in digital words by a proper ADC (represented by the $Q(\cdot)$ function of Figure 9) operating at a sub-Nyquist rate⁶.

Another group of works [50], [52] assume to operate directly on *digital* input signals. This approach has recently been receiving increasing attention, and aims at using CS as an early digital processing stage replacing complex and expensive (either in terms of required energy or hardware resources) classic compression algorithms. The corresponding architecture is shown as the “digital” case in Figure 9. The vector \mathbf{x} is made of digital words after windowing, sampling and quantizing the input signal $x(t)$. In order to compute y , it is enough to process \mathbf{x} with a common digital MAC architecture. Even if, in this case, the measurement y is already a digital quantity that can be delivered “as is” to the reconstruction algorithm, it is a common practice to apply an additional re-quantization function (such as the $Q'(\cdot)$ in the figure) to ensure, for example, a better adaptation to the statistics of y .

B. Multiplication by \mathbf{a}_k

Notwithstanding the actual implementation as a multiply-and-integrate [47], [48], or as multiply-and-accumulate stage [37], [49]–[51], [53], one of the main difficulties in realizing a CS signal acquisition stage is multiplying the input signal by the sensing sequence/function. In fact, a multiplier is one of the most complicated circuital block in a signal processing chain, both in the analog and in the digital domain.

To tackle this issue, almost all the considered works constrains the elements of vectors \mathbf{a}_k to assume a very

limited number of values. In [37], [47]–[49], it is required that $\mathbf{a}_k \in \{-1, +1\}$. The advantage of this approach is clear: the multiplier block can be replaced by a simple sign inversion circuit. More specifically, in the analog domain, and assuming a differential encoding for $x(t)$ [37], [47]–[49], [51], a few pass transistors capable of exchanging the $x^+(t)$ and $x^-(t)$ line are enough to perform multiplication by -1 . In the digital domain, the solution is similarly simple since a straightforward two’s complement allows a multiplication by -1 . The multiplication by $+1$ is, of course, trivial in both cases.

Another possible solution is to ask that $\mathbf{a}_k \in \{0, +1\}$ [50], [51], [53]. In this case the situation is even simpler, since the multiplication by $+1$ or 0 is simply achieved by allowing the input signal to be summed/integrated or by disconnecting it from the rest of the circuit, respectively.

When multiplication by an arbitrary value is desired, the resulting circuit complexity is expected to substantially increase and several authors have proposed remedies to cope with this. As an example, in the discrete-time analog input signal case, the authors of [49] describe a solution to achieve the multiplication by a 6-bit integer value at virtually no cost in terms of energy. More specifically, instead of relying on a simple switched capacitor integrator based on two capacitors such that shown in the “analog discrete-time” case of Figure 9, they replace C_s with a 5-bit C-2C split capacitor array circuit typically used in digital-to-analog converter. The effect is that only a part (that is proportional to the 5-bits control value) of the charge accumulated on the C-2C split capacitor array is transferred to the C_I , thus performing at the same time both a multiplication and the integration without any additional active device. The 6-th bit of the control word is used as sign bit, and decides if the signal to be integrated is $x(t)$ or $-x(t)$ by exchanging the $x^+(t)$ and $x^-(t)$ differential lines.

C. Time Continuity

In the windowing approach illustrated so far, the input signal $x(t)$ is sliced with respect to contiguous and non overlapping time intervals of length T_w . From a circuital point of view, let us refer again to Figure 9 and consider the time interval $I^{(l)}$. The measurement $y^{(l)}$ is computed by considering the input signal slice $x^{(l)}(t)$ and \mathbf{a} . At the end of $I^{(l)}$, $y^{(l)}$ is available, and can be converted into a digital word (or requantized assuming a digital

⁶While the Nyquist rate is defined as n/T_w , with this solution the ADC is working at a rate given by $1/T_w$, or m/T_w in case a single shared ADC is used to convert all m measurements.

Adapted CS is definitely worth pursuing whenever designing the low-resources, autonomous, ubiquitous sensing subsystems that will be the backbone of future IoT applications.

architecture). After that, the integrator circuit have to be reset in order to be ready to start the computation of a new measurement $y^{(l+1)}$. Note that these two operations (conversion to digital word/requantization and reset) may require a non-negligible amount of time.

Yet, at the same time instant when $I^{(l)}$ ends, $I^{(l+1)}$ starts and all the aforementioned processes need to be repeated on the successive slice $x^{(l+1)}(t)$ of the input signal to compute $y^{(l+1)}$. While it is reasonable to assume that both $y^{(l)}$ and $y^{(l+1)}$ should be computed by the same hardware block, it is straightforward to understand that the two above requirements are conflicting: *i*) a certain amount of time is needed for the hardware block to be ready for start the computation of the new measurement, and *ii*) the computation of the new measurement should start immediately after the end of the elaboration of the previous one.

While the solution for a digital architecture is trivial (a latch is enough to store the accumulated value so that the multiply-and-accumulate block is ready for the next computation), the situation is more complicated when considering analog hardware. In the latter case, a complex (and energy-hungry) analog sample/hold should in principle be required. To avoid it, [48] and [37] propose two similar solutions to be applied to the continuous-time and the discrete-time model, respectively.

Referring to the “analog continuous-time” case of Figure 9, in [48] the proposed multiply-and-integrate block is composed by a single multiplication block and by two integration paths. When the first block is integrating, the second one is disconnected from the multiplier and is working as a sample/hold block. This allows enough time to the cascade circuit to digitize the results, and also to clear the charge accumulated on C_f before starting a new integration. At the end of the time window, the role of the two paths is exchanged: the first one works as a sample/hold, while the second path starts a new integration phase for computing the next measurement.

An even simpler solution is presented in [37], where the proposed design is based on a switched capacitor architecture. Referring to the circuit sketched in the “analog discrete-time” case of Figure 9, the authors created two integration paths by replicating only the feedback capacitors C_f , while all other element (the multiplier, C_s and the active amplifier) are shared. The working principle is exactly the same as in the previous case: when the first C_f is used for computing the actual measurement, the second

C_f is sampling the previous measurement and may be connected to the cascading analog-to-digital converter, leaving enough time for the conversion and for removing the charge accumulated on it. At the end of each time window, the role of the two capacitors is exchanged. Note also that the further advantage of this solution is that no active (and so, energy consuming) devices are replicated.

D. Saturation

Independently of the architecture, measurements must be quantized/requantized before dispatching them. Unfortunately, such an operation may lead to saturation problems. Even if this has been rarely considered, it is a severe issue both for analog and digital CS implementations.

Since $y = \sum_{k=0}^{n-1} \mathbf{a}_k \mathbf{x}_k$, and assuming a large n (or more precisely, assuming that the number of terms $\mathbf{a}_k \mathbf{x}_k \neq 0$ is large), the central limit theorem can be applied to the sum resulting into y . As a consequence, the distribution of the result is expected to be approximately Gaussian, so that y may indeed assume very large values, while the majority of the observed cases will be practically located around the mean value.

This is an important issue for a twofold reason: *i*) the applied quantization function is uniform, i.e., all quantization steps have the same size, and *ii*) the conversion range is limited by an upper and a lower threshold, which identify the interval where conversion is correctly preformed, while outside it saturation occurs.

When an analog CS architecture needs to be implemented, the two above mentioned quantization thresholds must carefully be selected. In fact, it is obvious that using very different values can decrease (ideally, down to zero) the probability of a saturation event. This has however the drawback, due to the large quantization step, to increase the quantization error and reduces the reconstruction quality. Conversely, making the values of the two thresholds closer to each other results in a lower quantization error, but increases to a non-negligible value the probability of a saturation event.

A similar problem has to be considered also when computing y by means of a digital multiply-and-accumulate block. Unless a complex and non-efficient floating point representation is used, a high number of bits in the representation of y will result in negligible probability of saturation. The drawback is the non-efficient coding, since the most significant bits will hardly ever be used. It is worth stressing that a non-efficient coding of

measurements is actually a very serious problem, since it is in contrast with the ambition of CS to work as an efficient compression algorithm.

As an additional problem, saturation may actually be observed at *any time* in the computation of y . Let us define the succession of values

$$y[j] = \sum_{k=0}^j \mathbf{a}_k \mathbf{x}_k, \quad j = 0, 1, \dots, n-1 \quad (10)$$

with $y = y[n-1]$. This is the sequence of all intermediate partial sums that lead to y . Considerations similar to those mentioned above for y , hold also for each $y[j]$. When analog hardware is the choice, the integrator computing (10) may saturate (i.e. compromising the correct operation of the integrator in its linear region). Similarly, in a digital architecture, the multiply-and-accumulate block may overflow. In both cases, the outcome of the computation (i.e., the final y) is unpredictable. Using this value for reconstructing the input signal leads to an error that will impair the signal reconstruction.

A workaround for this problem was first proposed in [55] and adopted in [37] for the “analog discrete-time” case, and can be easily extended to any other architecture. The authors added two analog comparators to the multiply-and-integrate block with the aim of checking whether $y[j]$, $\forall j \in \{0, 1, \dots, n-1\}$ is in a safe range of linearity of the integrator block, defined by an upper threshold y_{sat}^+ and a lower one y_{sat}^- . As soon as this region is left, the time step \hat{j} is recorded along with the fact that the threshold being reached is y_{sat}^+ or y_{sat}^- .

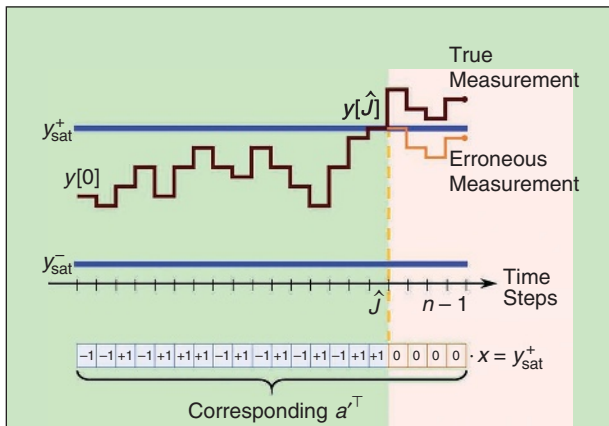


Figure 10. During the computation of a generic measurement y , when the intermediate accumulated value $y[j]$ leaves the safe interval $[y_{\text{sat}}^-, y_{\text{sat}}^+]$, a non-linear phenomenon occurs (saturation, overflow, etc.). In this case, the final accumulated value may be different from the expected one. Stopping the integration at time step \hat{j} when the safe region is left is a smart solution to get a non-erroneous measurement.

These data are transmitted to the reconstruction algorithm instead of the corrupted measurement.

More specifically, it is reasonable to assume that the expected value of each step $\mathbf{a}_k \mathbf{x}_k$ is small with respect to the integrator linearity range. In this way, the probability of a saturation event would be limited even for n large. As a consequence, we have either

$$\sum_{k=0}^{\hat{j}} \mathbf{a}_k \mathbf{x}_k \approx y_{\text{sat}}^- \quad \text{or} \quad \sum_{k=0}^{\hat{j}} \mathbf{a}_k \mathbf{x}_k \approx y_{\text{sat}}^+ \quad (11)$$

By introducing a sensing vector $\mathbf{a}' \in \mathbb{R}^n$ defined as

$$\mathbf{a}' = [\mathbf{a}_0, \mathbf{a}_0, \dots, \mathbf{a}_{\hat{j}}, 0, \dots, 0]^T$$

the two expressions in (11) can be written as $\mathbf{a}'^T \mathbf{x} \approx y_{\text{sat}}^-$ or $\mathbf{a}'^T \mathbf{x} \approx y_{\text{sat}}^+$, respectively, and can be used in the reconstruction algorithm to replace the erroneous $y = \mathbf{a}^T \mathbf{x}$. This approach is schematically represented in Figure 10.

The advantage of this solution with respect to the simple approach where measurements characterized by a saturation event are marked as invalid and not used in the reconstruction algorithm [56] can be explained by considering that the philosophy underlying CS is to reconstruct the input signal with the minimum amount of information. Accordingly, being able to recover even a small quantity of information from saturated measurements is an advantage. The authors of [37] showed that, using this approach, when a small ratio of measurements present saturation, it is still possible to recover the input signal with the same quality one get when no saturation events occur. Furthermore, they also showed that when up to 60% of the measurements are characterized by a saturation event, it is still possible to reconstruct the input signal with an almost negligible drop in performance.

E. Generation of Sensing Sequences

The generation of \mathbf{a} appears as a straightforward operation in a CS-based system. Nevertheless, when dealing with a practical CS systems implementation, this operation surprisingly requires appreciable care.

While in test prototypes it is commonly allowed to externally generate and load the sensing sequences [37], [47], any IoT CS-based not must have the elements of \mathbf{a} available on-chip. With respect to this, it is immediate to conclude that storing all the sensing sequences in an internal memory is in general not an option. In fact, referring for instance to [49] where $n = 256$, $m = 64$, and each entry of the sensing matrix is a 6-bit quantized value, storing all different elements of all vectors \mathbf{a} would require 100-Kbit of dedicated memory, something that should be avoided in the implementation of an analog circuit. So the path to follow is the on-chip generation of the sensing sequences.

Yet, as extensively shown in this paper, CS performance strongly depends on the choice of the acquisition sequences. We have seen that sensing sequences need to be randomly drawn or generated by adopting one of the discussed approaches. While the complexity of the second solution is obvious, the first case may present drawbacks when using a simple linear feedback shift register (LFSR) due to the low quality of the generated stream. The problem is relevant, in particular, if the number of channels is high, and so the number of different elements in \mathbf{a} to be generated at the same time.

While in [48], [51] the generation of sequences \mathbf{a} is achieved by a simple LFSR with no additional details, in [49] a complex Fibonacci—Galois 384-bit LFSR is designed. Basically, 64 6-bit Fibonacci LFSRs have been integrated into the circuit, each one generating a different \mathbf{a} . Then, the 64 LFSRs are further randomized by dithering their less significant bits in a Galois fashion, each LFSR using the most significant bits of another stage. An external trigger signal enables a 384-bit seed load at the beginning of each integration window⁷.

A completely different problem was instead faced in [47]. The proposed integrated circuit is a sub-Nyquist sampler for a 2 GHz bandwidth input signal. The circuit has a continuous-time analog architecture, and uses PAM sampling signal $a(t)$ obtained from antipodal sequences \mathbf{a} , where the multiplication by $a(t)$ is simply achieved by exchanging the differential lines of the differential input signal. Due to the 2 GHz input signal bandwidth, the \mathbf{a}_k symbols must be generated at a rate equal to 4 Gbit/s. The use of an internal serial memory for storing the \mathbf{a} vector, built upon a programmable shift register, even with all its implementation drawbacks, has been found to be the only solution allowing versatility at this speed.

The problem of the efficient generation of the elements of \mathbf{a} has also been considered in [53]. The authors propose a simple and deterministic algorithm to generate binary vectors \mathbf{a} (i.e., $\mathbf{a}_k \in \{0, 1\}$) that, once collected into the sensing matrix \mathbf{A} , ensures that *i)* \mathbf{A} satisfies the theoretical requirements for input signal reconstruction at the decoder side; and *ii)* \mathbf{A} is easily obtained with a finite state machine.

The method proposed in [53] relies on the quasi-cyclic array code based binary matrix framework. In particular, the authors aim to utilize the parity-check matrices of array codes and their submatrices to construct \mathbf{A} . In more details, let us indicate with \mathbf{I}_q the

$q \times q$ identity matrix, and \mathbf{P}_q the $q \times q$ cyclic permutation matrix defined as

$$\mathbf{P}_q = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ 1 & 0 & 0 & \cdots & 0 \end{bmatrix}$$

Given an integer r , the sensing matrix \mathbf{A} is the $rq \times q^2$ binary matrix given by

$$\mathbf{A} = \begin{bmatrix} \mathbf{I}_q & \mathbf{I}_q & \cdots & \mathbf{I}_q \\ \mathbf{I}_q & \mathbf{P}_q & \cdots & \mathbf{P}_q^{q-1} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{I}_q & \mathbf{P}_q^{r-1} & \cdots & \mathbf{P}_q^{(r-1)(q-1)} \end{bmatrix}$$

According to [53], the proposed approach shows comparable recovery performance for EEG and spike data compression with respect to standard approach at a reduced hardware complexity.

F. The Spatio-Temporal Approach

In the works [50], [51] authors consider a multichannel EEG recording as input. A multichannel signal may be modeled as an array $\mathbf{x}(t)$ composed of p real functions, with $\mathbf{x}: \mathbb{R} \mapsto \mathbb{R}^p$. By windowing it and sampling it at rate T_w/n , we get for each $I^{(l)}$, a slice of signal represented by a $p \times n$ matrix, that can be easily unrolled to get a $p \times n$ vector. The standard CS framework can then be applied to this vector with no other modification.

Indeed, a spatio-temporal approach may lead to several advantages with respect to a standard approach, since it make possible to exploit the input signal features in two different domains (i.e. spatial and temporal one).

This is an open research topic. Yet, by limiting ourselves to a pure circuital level consideration, it interesting to see how in [51] this model is used to reduce the hardware complexity of $y = \mathbf{a}^\top \mathbf{x}$. In fact, at each time step, a number of measurements is computed as a linear combination of the samples coming from all input signal channels sampled at that time step. Mathematically, at time step k , we get the generic measurement

$$y = \sum_{j=0}^{p-1} \mathbf{a}_j x^{(j)} \left(k \frac{T_w}{n} \right) \quad (12)$$

Then, all measurements generated at the k -th time step are collected by the reconstruction algorithm and joined to all measurements generated for all other time steps belonging to $I^{(l)}$. During reconstruction, both sparsity (on the time domain) and correlation (on the spatial domain) are used to improve the input signal reconstruction quality.

Computing measurements with a multiply-and-accumulate operation in the spatial domain only as in (12) has a twofold advantage.

⁷Note that, even if [49] is the only work where the elements of each \mathbf{a} are the approximations of real quantities, the authors considers only uniformly distributed random values due to the complexity of generating a Gaussian distribution at hardware level.

On the one hand, this avoids the time continuity problem described so far. At a generic time step k the input signal is sampled, and each sample is multiplied by \mathbf{a}_j and accumulated to get y as in (12). The measurements have to be quantized and dispatched before the end of the time step. This approach imposes time constraints tighter with respect to a standard approach and due to the necessity to deal at the same time with p different input signals (the time available for all the required operations is T_w/n instead of T_w). However, at the end of the time windows all measurements have already been converted and dispatched, and no additional actions are required between the end of a time windows and the beginning of the next one.

On the other hand, this approach makes the computation of y independent of the length of T_w . As observed in [37], a T_w that is too long (that is actually a common situation for biomedical signals such as ECG or EEG) may lead to leakage problems in analog implementation due to the discharge of the capacitors. In the light of this, an architecture where performance of the integrator is independent of T_w is a sure advantage.

G. Dynamic CS Approaches

In many cases, it may be useful to tune some parameters of a CS system on the particular input signal. For example, in biomedical signal acquisition, the dictionary \mathbf{D} used for reconstruction can be trained on the particular patient for improving performance. The training phase, however, cannot be done by using compressed measurements, but needs to be established before the starting of the CS operating mode.

Such an approach is considered in [50]. The interesting aspect from the circuital point of view is that the designed system works with a feedback signal generated by the reconstruction algorithm capable of enabling or disabling the CS operating mode. Initially, the CS mode is disabled (i.e., the device is working as a standard Nyquist-rate converter) and the uncompressed input EEG signal is sent to the receiver side which analyses it. When enough data is collected to allow a good estimation of a trained dictionary, a signal is sent to the acquisition device to start the CS operating mode.⁸

A different case is taken into account in [52], where no CS architectures are considered. Indeed, the design of a low-power companion chip capable of detecting features of the input signal is presented. The aim of the work is to identify the type of the input signal among many possible biosignals. In this way, it should be possible to adapt pa-

rameters of the CS (for example, the number of measurements m , the time windows T_w , the number of samples n per time window, and so on) to that of the input signal, with advantages in terms of reconstruction quality and/or energy required to sample the input signal.

VIII. Conclusion

CS is often thought of as a technique in which adaptation cannot play a significant role. Yet, a careful scan of the literature reveals that many methods have been developed to adjust either the encoding or the decoding side of CS depending on the class of signals that has to be acquired. Moreover, every hardware implementation has to adapt the general paradigm to cope with realization constraints or resource budgets.

Our review shows that these designs are able to yield significant improvements that cannot be predicted by classical theoretical guarantees dealing with worst-case analysis.

Yet, the possibility of substantially increasing the compression ratio while obeying to the same requirements in terms of quality of the recovered signal, is a key point to allow the effective introduction of CS in application in which resources must be carefully administered. From this point of view, adapted CS is definitely worth pursuing whenever designing the low-resources, autonomous, ubiquitous sensing subsystems that will be the backbone of future IoT applications.



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⁸ Note also that the trained dictionary characterizes the first of two phases of the proposed decoding procedure. Here, the main signal shape is approximately reconstructed by using a single atom from the trained dictionary. In the second phase, signal details are recovered using Daubechies wavelet transformation as sparsity basis.

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ICECS is an international conference dedicated to circuits and systems, held annually in Region 8 (EU, Africa and Middle-east). The 27th edition of this IEEE Circuits and Systems Society Region 8 flagship conference will take place in Glasgow, Scotland, United Kingdom.

The scope of the conference will focus and not limited to:

- » Analog/mixed-signal/RF circuits
- » Biomedical and Bio-Inspired Circuits and Systems
- » EDA, Test and Reliability
- » Digital circuits and systems
- » Linear and Non-linear Circuits
- » Low-Power Low-Voltage Design
- » Microsystems
- » Neural networks, Machine and Deep Learning
- » Sensors and Sensing Systems
- » Signal Processing, Image and Video
- » VLSI Systems and Applications

To implement the above vision, this year's conference will highlight the following disruptive themes:

- » Society 5.0 - Human-centric Society
- » Sustainable Computing and Systems
- » Energy-aware Systems and Services
- » Nanosatellite and smart IoT
- » Smart Systems for Automotive
- » Lab-on-CMOS, Wearable and Implantable Devices

A selection of the top accepted papers will be invited to submit an extended version for Journals supported by IEEE Circuits and Systems Society.

SUBMISSIONS

The technical committee invites authors to submit 4-page papers in standard IEEE double-column format, including references, figures and tables, to clearly present the work, methods, originality, significance and applications of the techniques discussed. Accepted papers will be submitted for inclusion to IEEE Xplore.





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